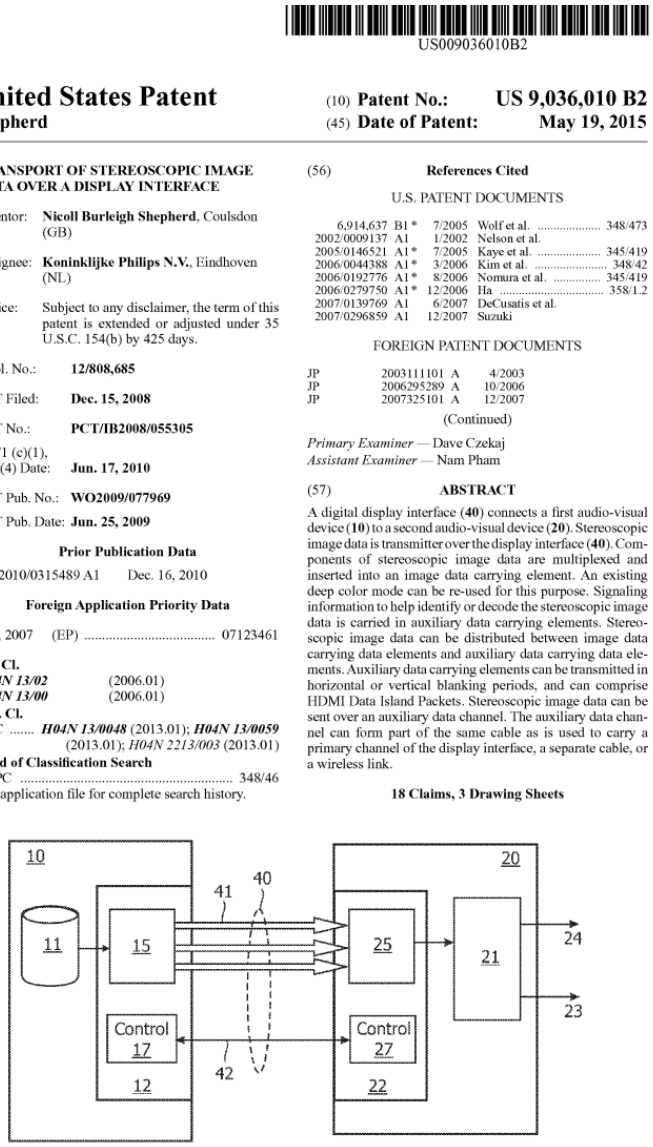
APPENDIX F

US 9,036,010

US 9,036,010

- Title: Transport of stereoscopic image data over a display interface



US009036010B2

(12) **United States Patent**
Shepherd

(10) **Patent No.: US 9,036,010 B2**
(45) **Date of Patent: May 19, 2015**

(54) **TRANSPORT OF STEREOSCOPIC IMAGE DATA OVER A DISPLAY INTERFACE**

(75) Inventor: **Nicoll Burleigh Shepherd**, Coulsdon (GB)

(73) Assignee: **Koninklijke Philips N.V.**, Eindhoven (NL)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 425 days.

(21) Appl. No.: **12/808,685**

(22) PCT Filed: **Dec. 15, 2008**

(86) PCT No.: **PCT/IB2008/055305**

§ 371 (c)(1),
(2), (4) Date: **Jun. 17, 2010**

(87) PCT Pub. No.: **WO2009/077969**

PCT Pub. Date: **Jun. 25, 2009**

(65) **Prior Publication Data**

US 2010/0315489 A1 Dec. 16, 2010

(30) **Foreign Application Priority Data**

Dec. 18, 2007 (EP) 07123461

(51) **Int. Cl.**
H04N 13/02 (2006.01)
H04N 13/00 (2006.01)

(52) **U.S. Cl.**
CPC ***H04N 13/0048*** (2013.01); ***H04N 13/0059*** (2013.01); *H04N 2213/003* (2013.01)

(58) **Field of Classification Search**
USPC 348/46
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,914,637 B1 * 7/2005 Wolf et al. 348/473
2002/0009137 A1 1/2002 Nelson et al.
2005/0146521 A1 * 7/2005 Kaye et al. 345/419
2006/0044388 A1 * 3/2006 Kim et al. 348/42
2006/0192776 A1 * 8/2006 Nomura et al. 345/419
2006/0279750 A1 * 12/2006 Ha 358/1.2
2007/0139769 A1 6/2007 DeCusatis et al.
2007/0296859 A1 12/2007 Suzuki

FOREIGN PATENT DOCUMENTS

JP 2003111101 A 4/2003
JP 2006295289 A 10/2006
JP 2007325101 A 12/2007

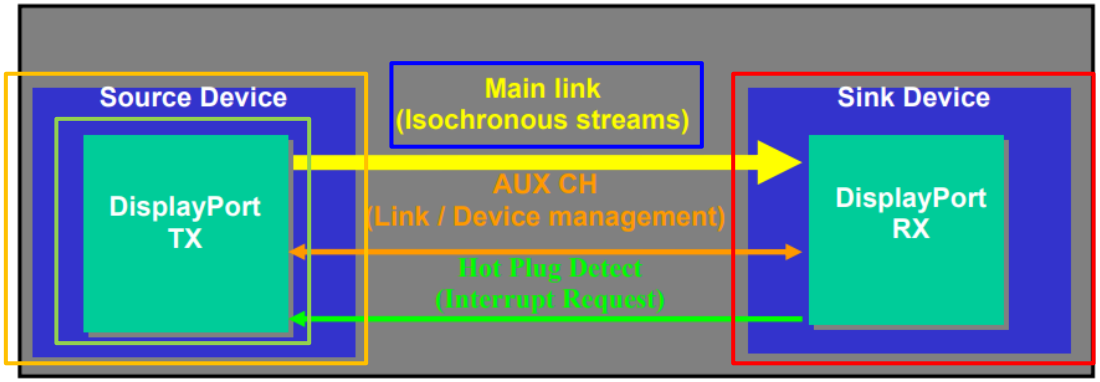
(Continued)

Primary Examiner — Dave Czekaj
Assistant Examiner — Nam Pham

(57) **ABSTRACT**

A digital display interface (**40**) connects a first audio-visual device (**10**) to a second audio-visual device (**20**). Stereoscopic image data is transmitter over the display interface (**40**). Components of stereoscopic image data are multiplexed and inserted into an image data carrying element. An existing deep color mode can be re-used for this purpose. Signaling information to help identify or decode the stereoscopic image data is carried in auxiliary data carrying elements. Stereoscopic image data can be distributed between image data carrying data elements and auxiliary data carrying data elements. Auxiliary data carrying elements can be transmitted in horizontal or vertical blanking periods, and can comprise HDMI Data Island Packets. Stereoscopic image data can be sent over an auxiliary data channel. The auxiliary data channel can form part of the same cable as is used to carry a primary channel of the display interface, a separate cable, or a wireless link.

18 Claims, 3 Drawing Sheets

Claim 1	VESA DisplayPort Standard v1.2
1. A digital display interface part, for use in a first audio-visual device, for supporting a digital display interface between the first audio-visual device and a second audio-visual device, the digital display interface having a known data carrying capacity for transmitting uncompressed pixel information, the interface part comprising:	**1.7 Overview of DisplayPort** A DisplayPort link consists of a main link, an auxiliary channel (AUX CH), and a Hot Plug Detect (HPD) signal line. **As shown in Figure 2-45: DisplayPort Data Transport Channels** below, the Main Link is a unidirectional, high-bandwidth and low-latency channel used below, the Main Link is a unidirectional, high-bandwidth and low-latency channel used to transport isochronous data streams such as uncompressed video and audio. The auxiliary channel is a half-duplex bidirectional channel used for link management and device control. The HPD signal also serves as an interrupt request by the Sink device. In addition, the DisplayPort connector for a box-to-box connection has a power pin for powering either a DisplayPort repeater or a DisplayPort-to-Legacy converter.  **Figure 1-1: DisplayPort Data Transport Channels**

Claim 1	VESA DisplayPort Standard v1.2
1. A digital display interface part, for use in a first audio-visual device, for supporting a digital display interface between the first audio-visual device and a second audio-visual device, the digital display interface having a known data carrying capacity for transmitting uncompressed pixel information, the interface part comprising:	**1.7 Overview of DisplayPort** A DisplayPort link consists of a main link, an auxiliary channel (AUX CH), and a Hot Plug Detect (HPD) signal line. **As shown in Figure 2-45: DisplayPort Data Transport Channels** below, the Main Link is a unidirectional, high-bandwidth and low-latency channel used below, the Main Link is a unidirectional, high-bandwidth and low-latency channel used to transport isochronous data streams such as uncompressed video and audio. The auxiliary channel is a half-duplex bidirectional channel used for link management and device control. The HPD signal also serves as an interrupt request by the Sink device. In addition, the DisplayPort connector for a box-to-box connection has a power pin for powering either a DisplayPort repeater or a DisplayPort-to-Legacy converter. **1.7.1 Make-up of the Main Link** The Main Link consists of one, two or four AC-coupled, doubly terminated differential pairs (called lanes). AC-coupling facilitates the silicon process migration since the DisplayPort transmitter and receiver may have different common mode voltages. Three link rates are supported, 5.4Gbps, 2.7Gbps and 1.62Gbps per lane. All enabled lanes must be operating at the same link rate. The link rate is decoupled from the pixel rate. The pixel rate is regenerated from the link symbol clock using the time stamp values M and N. The capabilities of the DisplayPort transmitter and receiver, and the quality of the channel (or a cable) will determine whether the link rate is set to 5.4Gbps, 2.7Gbps or 1.62Gbps per lane.

Claim 1	VESA DisplayPort Standard v1.2
an input for receiving image data;	

2.2.1 Main Stream to Main Link Lane Mapping in the Source Device

The Main Link must have one, two, or four lanes, with each lane capable of transporting eight bits of data per link symbol clock (LS_Clk). Main stream data (the uncompressed video stream) must be packed, stuffed, framed and, optionally, multiplexed with secondary-data and inter-lane skewed before it is handed over to the PHY layer after the Link Layer data mapping for transport over the main link. The stream data must enter the link layer at the original stream clock (Strm_Clk) rate and must be delivered to the PHY layer at the LS_Clk rate after this mapping.

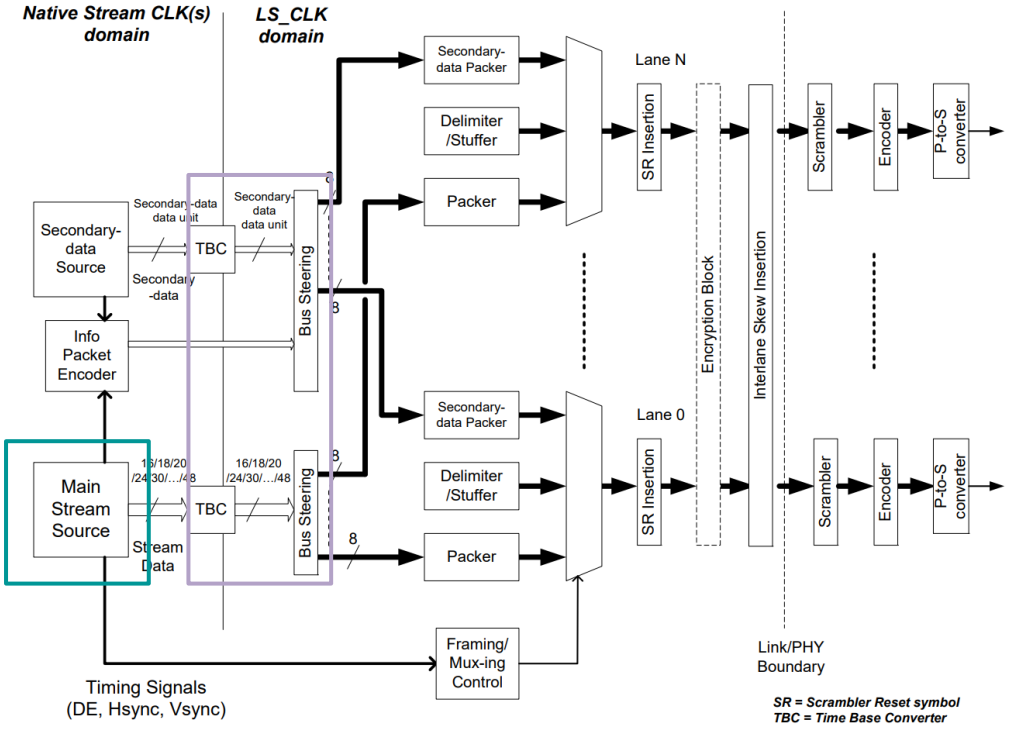


Figure 2-8: High Level Block Diagram of DP uPacket TX Main Link Data Path

Claim 1	VESA DisplayPort Standard v1.2
an input for receiving image data;	

1.7.4 Layered, Modular Architecture

Figure 1-2: shows the layered architecture of DisplayPort.

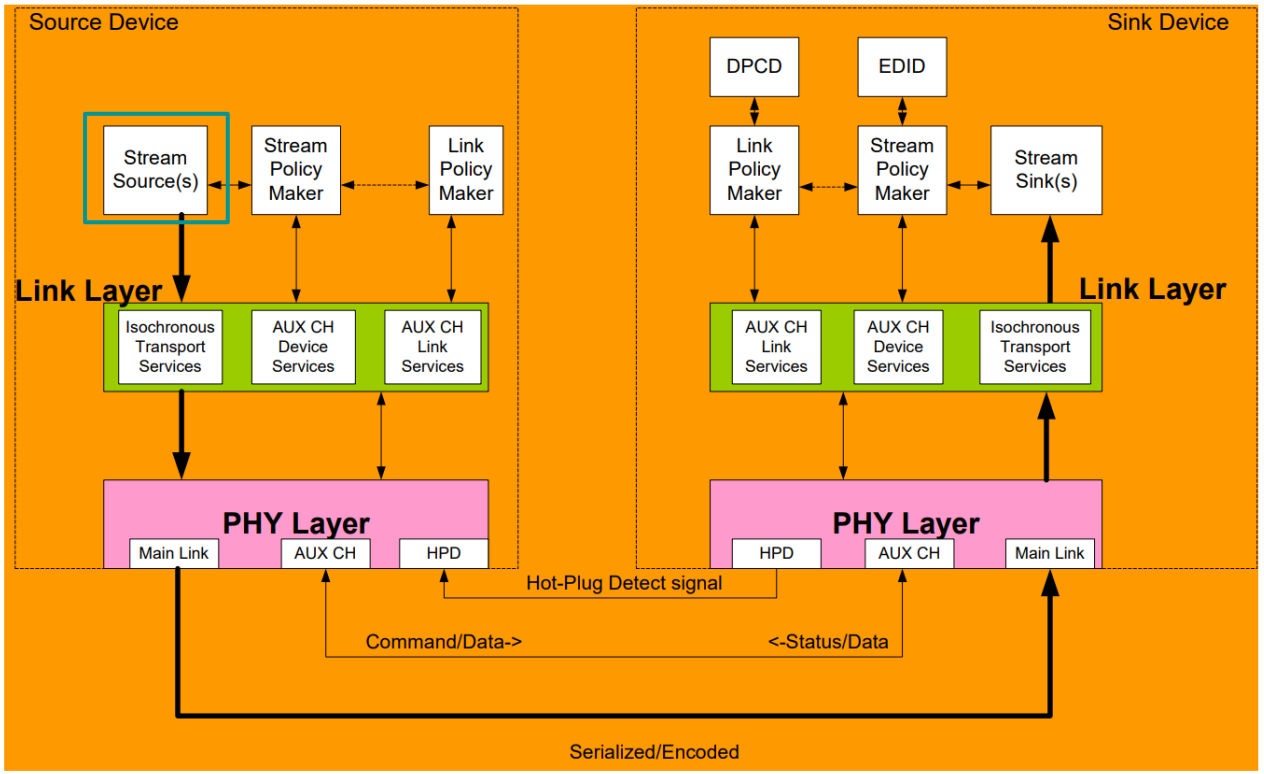


Figure 1-2: Layered Architecture

Claim 1	VESA DisplayPort Standard v1.2
a formatter arranged to format the data for transport over the interface, wherein the formatter, in accordance with signal information received from the second audio-device, is operable in:	

2.2.1 Main Stream to Main Link Lane Mapping in the Source Device

The Main Link must have one, two, or four lanes, with each lane capable of transporting eight bits of data per link symbol clock (LS_Clk). Main stream data (the uncompressed video stream) must be packed, stuffed, framed and, optionally, multiplexed with secondary-data and inter-lane skewed before it is handed over to the PHY layer after the Link Layer data mapping for transport over the main link. The stream data must enter the link layer at the original stream clock (Strm_Clk) rate and must be delivered to the PHY layer at the LS_Clk rate after this mapping.

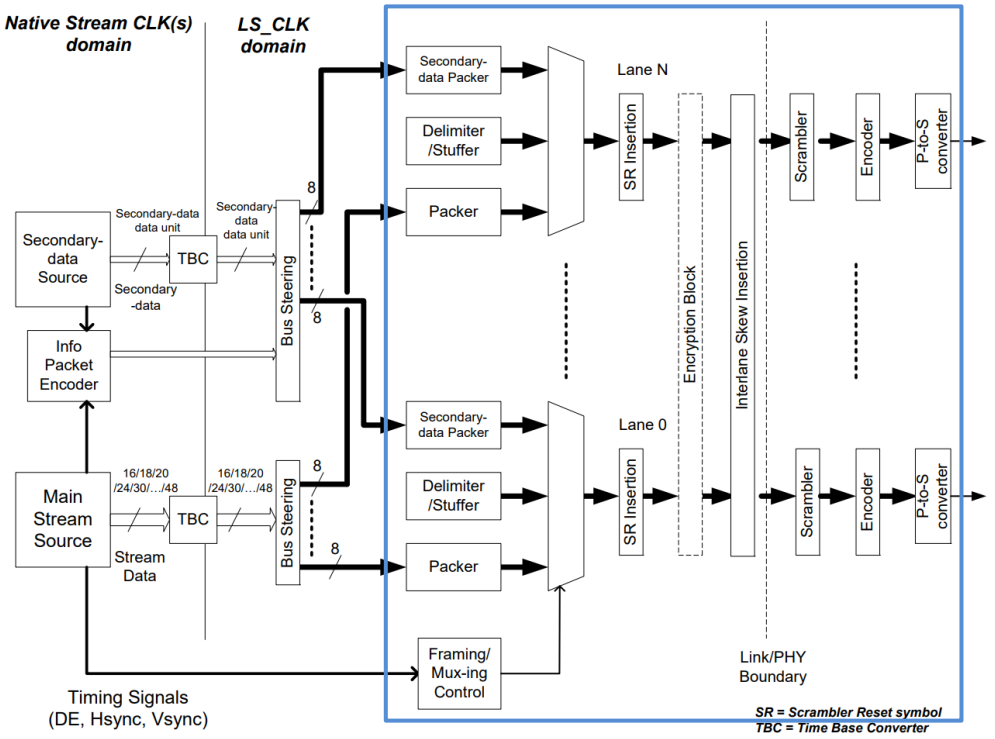


Figure 2-8: High Level Block Diagram of DP uPacket TX Main Link Data Path

Claim 1	VESA DisplayPort Standard v1.2
a formatter arranged to format the data for transport over the interface, wherein the formatter, in accordance with signal information received from the second audio-device, is operable in:	

2 Link Layer

2.1 SST Mode Introduction

This section describes the services provided by the link layer of DisplayPort in SST (single stream transport) mode. (Those sub-sections in this section that are applicable to both SST and MST modes are explicitly noted in the sub-section titles.) These services are:

- Isochronous transport services over the main link

  The isochronous transport services, based on a micro-packet architecture, maps the video and audio streams onto the Main Link symbols with a set of rules, (explained in Section 2.2), so that the streams can be correctly re-constructed into the original format and time base in the Sink device.

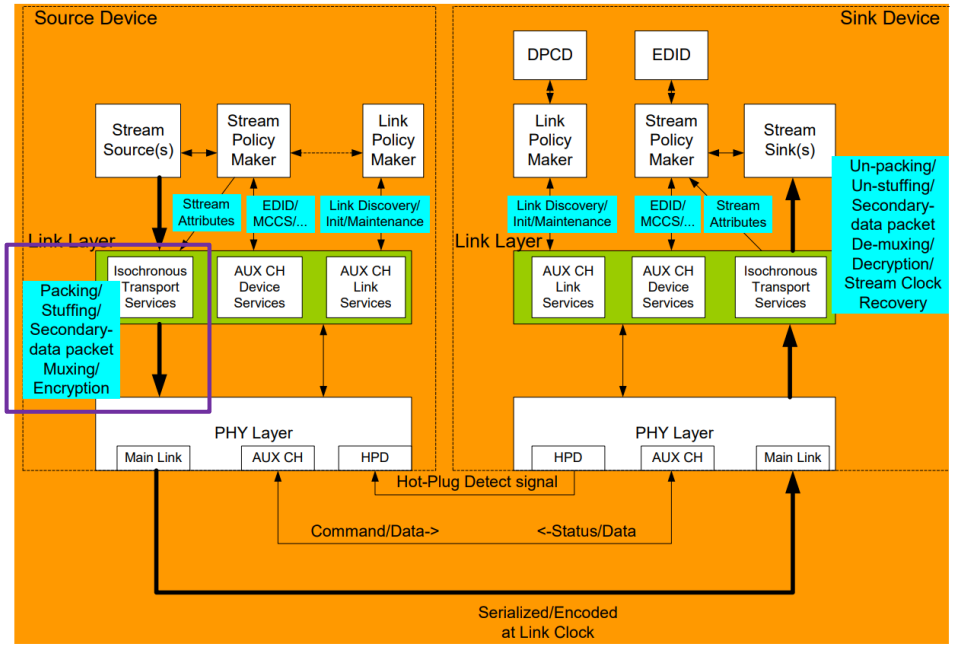


Figure 2-1: Overview of Link Layer Services

Claim 1	VESA DisplayPort Standard v1.2
a formatter arranged to format the data for transport over the interface, wherein the formatter, in accordance with signal information received from the second audio-device, is operable in:	

2 Link Layer

2.1 SST Mode Introduction

This section describes the services provided by the link layer of DisplayPort in SST (single stream transport) mode. (Those sub-sections in this section that are applicable to both SST and MST modes are explicitly noted in the sub-section titles.) These services are:

- Link and device management services over the AUX CH

  Link services are used for discovering, configuring, and maintaining the link. The AUX CH read/write access to DPCD (DisplayPort Configuration Data) address is used for these purposes. Device services support device-level applications such as EDID read and MCCS control. In addition, the AUX CH may be used for optional content protection.

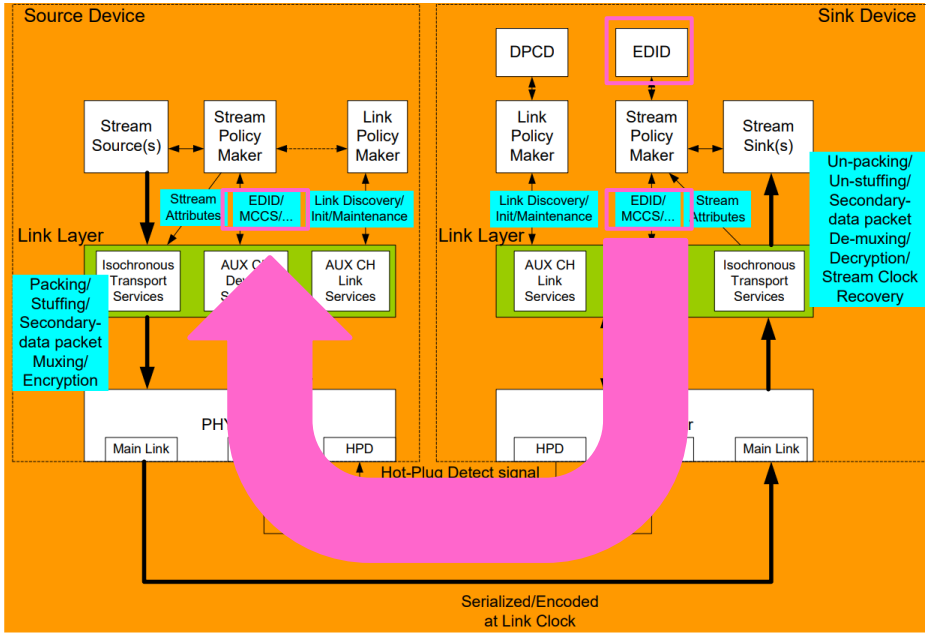


Figure 2-1: Overview of Link Layer Services

Claim 1	VESA DisplayPort Standard v1.2

a formatter arranged to format the data for transport over the interface, wherein the formatter, in accordance with signal information received from the second audio-device, is operable in:	**2.3.3 Policy Maker AUX CH Management**
	There are multiple applications and services that initiate AUX transactions. Some examples are:
	• AUX Link Services
	  ○ Link capability read
	  ○ Link configuration (training)
	  ○ Link status read
	• AUX Device Services
	  ○ EDID read
	  ○ MCCS (Monitor Command and Control Set) control
	
	2.9.1 Stream Transport Initiation Sequence
	The Stream Source Policy Maker, before transport initiation, must take the following actions:
	• Read EDID from the Sink device
	• Set stream attributes for Main Stream attribute data and CEA 861-C InfoFrame generation
	• Optionally (recommended), get the following information from the Link Policy Maker
	  ○ Link configuration: Total link bandwidth
	  ▪ To avoid oversubscription of the link bandwidth
	  ○ RX capability: Number and types of ports available in RX
	  ▪ To determine the number and types of streams that may be transported
	  ○ Link status: Synchronized? Excessive error symbols?
	  ▪ To make sure that the link is ready for transport

Claim 1	VESA DisplayPort Standard v1.2
a formatter arranged to format the data for transport over the interface, wherein the formatter, in accordance with signal information received from the second audio-device, is operable in:	

2.9.3.1 Address Mapping for Link Configuration/Management

Table 2-75 shows the DisplayPort address mapping for DPCD. The DPCD is byte addressed.

Table 2-75: Address Mapping for DPCD (DisplayPort Configuration Data)

DisplayPort Address	Definition	Read/Write over AUX CH
	Receiver Capability Field	
00000h	DPCD_REV : DPCD revision number Bits 3:0 = Minor revision number Bits 7:4 = Major revision number 10h for DPCD Rev.1.0 11h for DPCD Rev.1.1 12h for DPCD Rev 1.2 A DP device with uPacket RX with a DPCD Revision number of 1.2 and above must support GUID at DPCD Addresses 00030h ~ 0003Fh. Furthermore, a DP Sink device with DPCD Rev.1.2 with a stereo display capability support (as declared in EDID and Display ID) must support the handling of 3D Stereo in-band signaling using Video_Stream_Configuration (VSC) Packet. **Note:** The DPCD revision number does not necessarily match the DisplayPort version number.	Read Only

13 Appendix H: Protocol Support for 3D Stereo Display

13.2 3D Stereo Display Capability Declaration

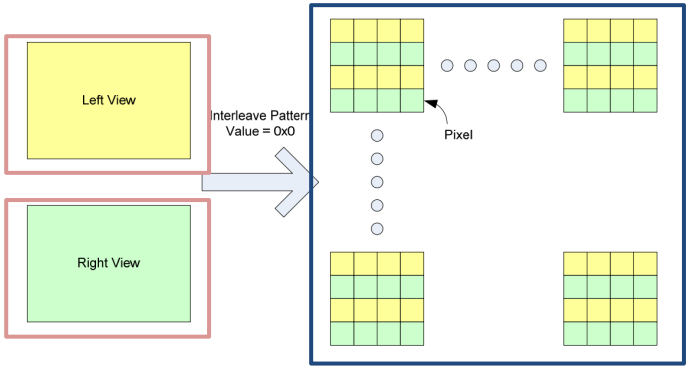
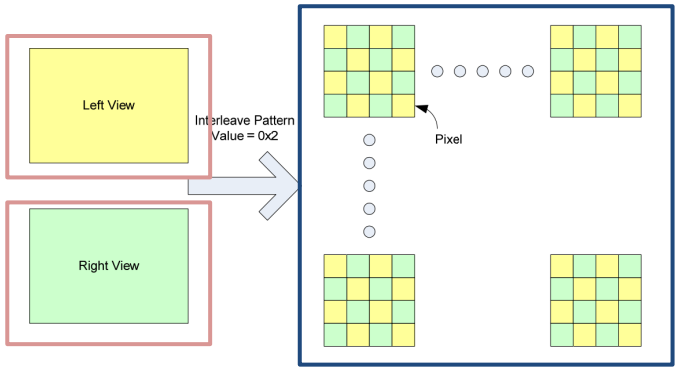
The 3D stereo capability can be exposed in EDID and DisplayID. A 3D stereo format is usually associated with specific timing and hence it is desirable to indicate which timings support 3D stereo format and which don't. Furthermore, for a given timing that supports 3D stereo format it is required to indicate which stereo format is supported. Both EDID and DisplayID have the ability to expose 3D stereo capability per timing, but DisplayID provides for a more efficient and flexible format declaration.

Claim 1	VESA DisplayPort Standard v1.2
a first mode to generate a stream of first data elements, said first data element comprising pixel data of a 2D image, at a data carrying capacity no greater than said known data carrying capacity; and,	**2.2.4 Main Stream Attribute Data Transport** This section describes the Main Stream attribute data that are transported for the reproduction of the main video stream by the Sink. The attribute data is sent once per frame during the vertical blanking period of the main video stream. Those attributes must be as follows: • Miscellaneous1 (MISC1, 8 bits) o Stereo video attribute (bits 2:1) ▪ 00 = No 3D stereo video in-band signaling done using this field, indicating either no 3D stereo video transported or the in-band signaling done using an SDP called Video_Stream_Configuration (VSC) Packet **2.2.5.6 Video_Stream_Configuration (VSC) Packet** A DP Source device may send 3D Stereo in-band signaling using VSC Packet by setting MSA Packet MISC1 field bits 2:1 to 00. **2.2.5.6.2 VSC Packet Payload** Table below shows the bit definitions of VSC Packet payload **Table 2-56: VSC Packet Payload** **DB0 bits 3:0 = Stereo Interface Method Code** | **DB0 bits 7:4 = Stereo Interface Method-Specific Parameter** 0 = Non Stereo Video | Must be set to 0x0

Claim 1	VESA DisplayPort Standard v1.2
a first mode to generate a stream of first data elements, said first data element comprising pixel data of a 2D image, at a data carrying capacity no greater than said known data carrying capacity; and,	**1.7.1 Make-up of the Main Link** The Main Link consists of one, two or four AC-coupled, doubly terminated differential pairs (called lanes). AC-coupling facilitates the silicon process migration since the DisplayPort transmitter and receiver may have different common mode voltages. The stream data is packed into "micro-packets" which are called "transfer units" in SST (Single Stream Transport) mode and MTP (Multi-stream Transport Packet) in MST (Multi-Stream Transport) mode. After the stream data is packed and mapped to main link, the packed stream data rate will be equal to or smaller than the link symbol rate of the main link. When it is smaller, stuffing symbols are inserted. **2.2.1.4 Symbol Stuffing and Transfer Unit** To avoid the oversubscription of the link bandwidth, the packed data rate must be equal to or lower than the link symbol rate. When the packed data rate is lower than the link symbol rate, the link layer must perform symbol stuffing. Stuffing symbols (both stuffing frame symbols and dummy data symbols) must be inserted in all lanes in the same LS_Clk cycle before inter-lane skewing. The dummy data symbols must be all 00h before scrambling. The dummy data symbols are inserted both between FS and FE, and between BS and BE.

Claim 1	VESA DisplayPort Standard v1.2
a second mode to generate a stream of second data elements which carry a multiplexed combination of components of a stereoscopic image, wherein said components of said stereoscopic image elements being transmitted in a first portion of said interface and in a second portion of said interface,	**2.2.4 Main Stream Attribute Data Transport** This section describes the Main Stream attribute data that are transported for the reproduction of the main video stream by the Sink. The attribute data is sent once per frame during the vertical blanking period of the main video stream. Those attributes must be as follows: • Miscellaneous1 (MISC1, 8 bits) ○ Stereo video attribute (bits 2:1) ▪ 00 = No 3D stereo video in-band signaling done using this field, indicating either no 3D stereo video transported or the in-band signaling done using an SDP called Video_Stream_Configuration (VSC) Packet

Claim 1	VESA DisplayPort Standard v1.2
a second mode to generate a stream of second data elements which carry a multiplexed combination of components of a stereoscopic image, wherein said components of said stereoscopic image elements being transmitted in a first portion of said interface and in a second portion of said interface,	**2.2.5.6 Video_Stream_Configuration (VSC) Packet** A DP Source device may send 3D Stereo in-band signaling using VSC Packet by setting MSA Packet MISC1 field bits 2:1 to 00. **2.2.5.6.2 VSC Packet Payload** Table below shows the bit definitions of VSC Packet payload **Table 2-56: VSC Packet Payload** **DB0 bits 3:0 = Stereo Interface Method Code** / **DB0 bits 7:4 = Stereo Interface Method-Specific Parameter** 1 = Frame/Field Sequential (Figure 6, illustrates the composited frame format as transmitted by the source) — **Frame/Field Sequential Type:** *Value 0x0:* Left & Right view indication based on the MISC1 bit 2:1 *Value 0x1:* Right when Stereo Signal = 1 *Value 0x2:* Left when Stereo Signal = 1 All other values for this field (0x3-0xF) are RESERVED for future use. 2 = Stacked Frame (Figure 7, illustrates the composited frame format as transmitted by the source) — **Stacked Frame Type:** *Value 0x0:* Left view is on top and right view on bottom All other values for this field (0x1-0xF) are RESERVED for future use. 3 = Pixel Interleaved — **Interleave Pattern Type:** For interleave pattern type 1 through 4, a 2x2 pattern

Claim 1	VESA DisplayPort Standard v1.2
a second mode to generate a stream of second data elements which carry a multiplexed combination of components of a stereoscopic image, wherein said components of said stereoscopic image elements being transmitted in a first portion of said interface and in a second portion of said interface,	**2.2.5.6 Video_Stream_Configuration (VSC) Packet** A DP Source device may send 3D Stereo in-band signaling using VSC Packet by setting MSA Packet MISC1 field bits 2:1 to 00.  **Figure 2-29: Interleave Pattern Corresponding to 2-way Interleaved Stereo where Right Image Pixels are on Even Lines**  **Figure 2-30: Interleave Pattern Corresponding to 2-way Interleaved Stereo where Right Image Pixels are on Even Lines**

Claim 1	VESA DisplayPort Standard v1.2
a second mode to generate a stream of second data elements which carry a multiplexed combination of components of a stereoscopic image, wherein said components of said stereoscopic image elements being transmitted in a first portion of said interface and in a second portion of said interface,	

2.2.5.6 Video_Stream_Configuration (VSC) Packet

A DP Source device may send 3D Stereo in-band signaling using VSC Packet by setting MSA Packet MISC1 field bits 2:1 to 00.

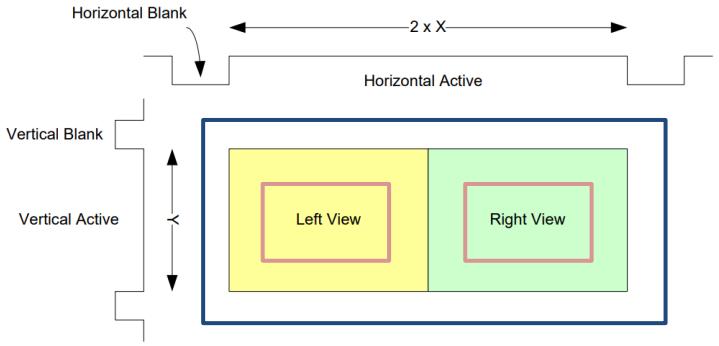


Figure 2-31: Interleave Pattern Corresponding to a Checkerboard Pattern with Alternating Left and Right Image Pixels

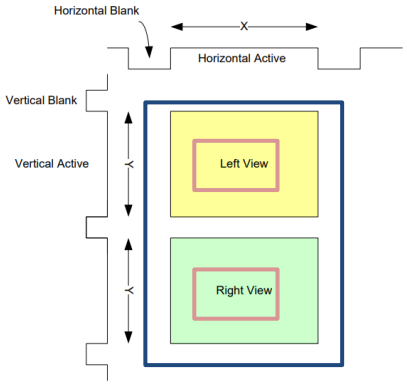


Figure 2-32: Field Sequential Stereo Format with Left View and Right View Indicated via MISC1 bits 2:1 Field of the MSA

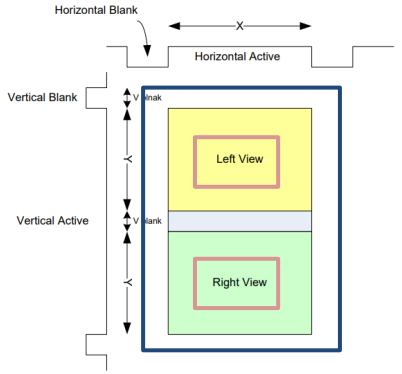
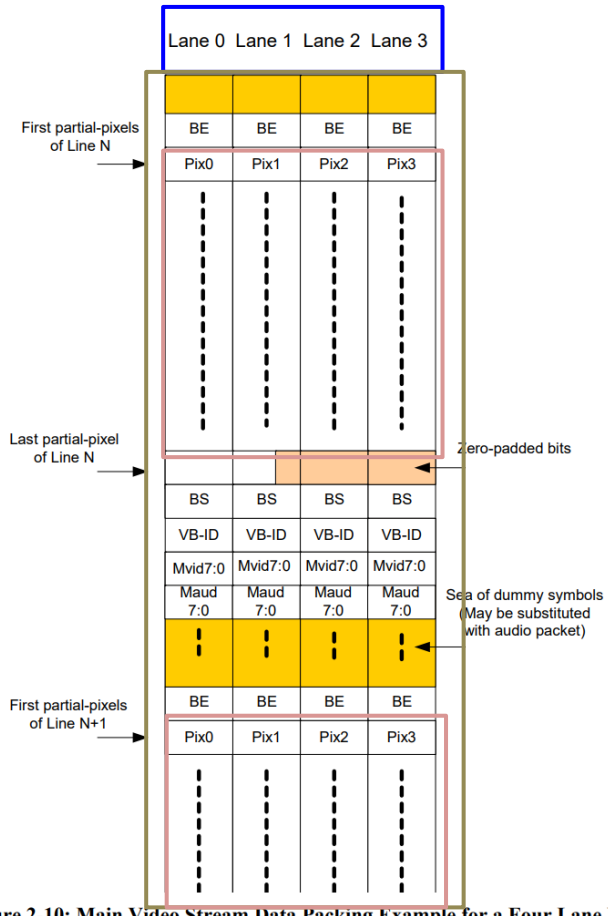
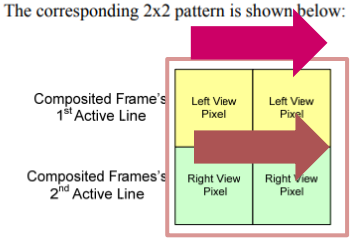
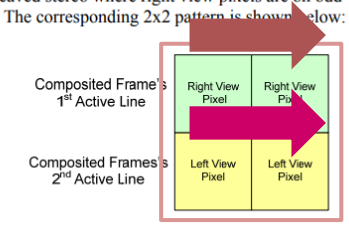
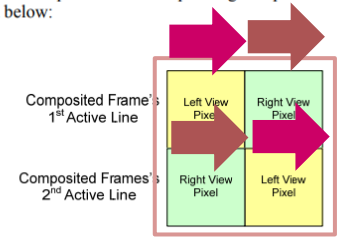
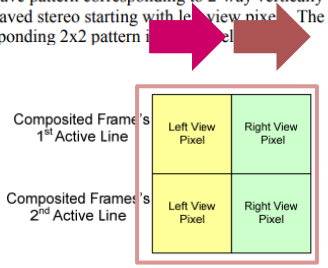
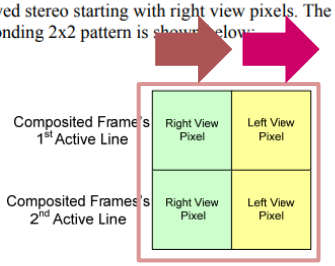
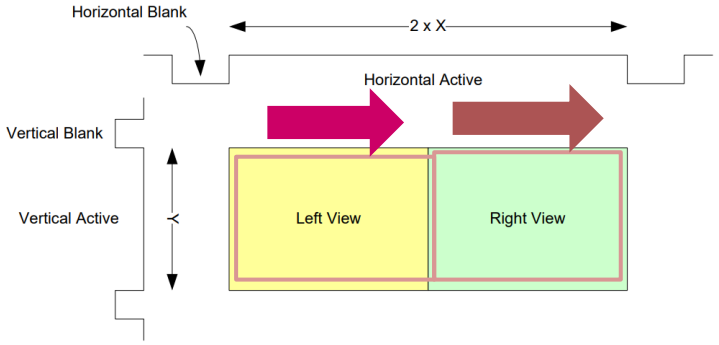
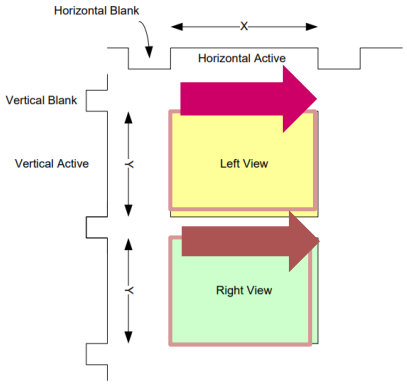
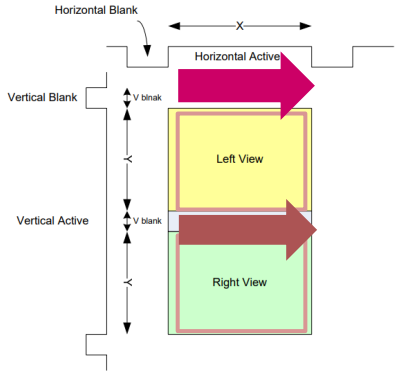


Figure 2-33: Stacked Top, Bottom Stereo Format with Left View on Top and Right View on Bottom

Claim 1	VESA DisplayPort Standard v1.2
a second mode to generate a stream of second data elements which carry a multiplexed combination of components of a stereoscopic image, wherein said components of said stereoscopic image elements being transmitted in a first portion of said interface and in a second portion of said interface,	**2.2.1.3 Main Video Stream Data Packing** The link layer must first steer pixel data in a pixel-within-lane manner as shown in Table 2-2. **Table 2-2: Pixel Steering into Main Link Lanes** <table><tr><th>Number of Lanes</th><th>Pixel Steering (N is 0 or positive integer)</th></tr><tr><td>4</td><td>Pixel 4N to lane 0 Pixel 4N+1 to lane 1 Pixel 4N+2 to lane 2 Pixel 4N+3 to lane 3</td></tr><tr><td>2</td><td>Pixel 2N to lane 0 Pixel 2N+1 to lane 1</td></tr><tr><td>1</td><td>All pixels to lane 0</td></tr></table>

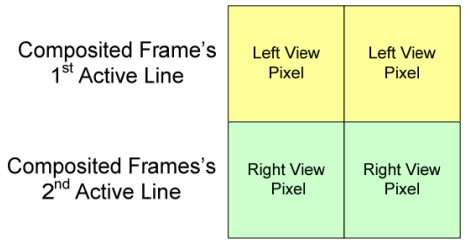
Claim 1	VESA DisplayPort Standard v1.2
a second mode to generate a stream of second data elements which carry a multiplexed combination of components of a stereoscopic image, wherein said components of said stereoscopic image elements being transmitted in a first portion of said interface and in a second portion of said interface,	 **Figure 2-10: Main Video Stream Data Packing Example for a Four Lane Main Link**

Claim 1	VESA DisplayPort Standard v1.2
a second mode to generate a stream of second data elements which carry a multiplexed combination of components of a stereoscopic image, wherein said components of said stereoscopic image elements being transmitted in a first portion of said interface and in a second portion of said interface,	**2.2.5.6 Video_Stream_Configuration (VSC) Packet** A DP Source device may send 3D Stereo in-band signaling using VSC Packet by setting MSA Packet MISC1 field bits 2:1 to 00. ***Value 0x0:*** Interleave pattern corresponding to 2-way horizontally interleaved stereo where right view pixels are on even lines. The corresponding 2x2 pattern is shown below:  ***Value 0x1:*** Interleave pattern corresponding to 2-way horizontally interleaved stereo where right view pixels are on odd lines. The corresponding 2x2 pattern is shown below:  ***Value 0x2:*** Interleave pattern corresponding to a checkerboard pattern with alternating left and right view pixels starting with left view pixel. The corresponding 2x2 pattern is shown below:  ***Value 0x3:*** Interleave pattern corresponding to 2-way vertically interleaved stereo starting with left view pixels. The corresponding 2x2 pattern is shown below:  ***Value 0x4:*** Interleave pattern corresponding to 2-way vertically interleaved stereo starting with right view pixels. The corresponding 2x2 pattern is shown below: 

Claim 1	VESA DisplayPort Standard v1.2
a second mode to generate a stream of second data elements which carry a multiplexed combination of components of a stereoscopic image, wherein said components of said stereoscopic image elements being transmitted in a first portion of said interface and in a second portion of said interface,	**2.2.5.6 Video_Stream_Configuration (VSC) Packet** A DP Source device may send 3D Stereo in-band signaling using VSC Packet by setting MSA Packet MISC1 field bits 2:1 to 00.  **Figure 2-31: Interleave Pattern Corresponding to a Checkerboard Pattern with Alternating Left and Right Image Pixels**  **Figure 2-32: Field Sequential Stereo Format with Left View and Right View Indicated via MISC1 bits 2:1 Field of the MSA**  **Figure 2-33: Stacked Top, Bottom Stereo Format with Left View on Top and Right View on Bottom**

Claim 1	VESA DisplayPort Standard v1.2
a second mode to generate a stream of second data elements which carry a multiplexed combination of components of a stereoscopic image, wherein said components of said stereoscopic image elements being transmitted in a first portion of said interface and in a second portion of said interface,	

Value 0x0:
Interleave pattern corresponding to 2-way horizontally interleaved stereo where right view pixels are on even lines. The corresponding 2x2 pattern is shown below:



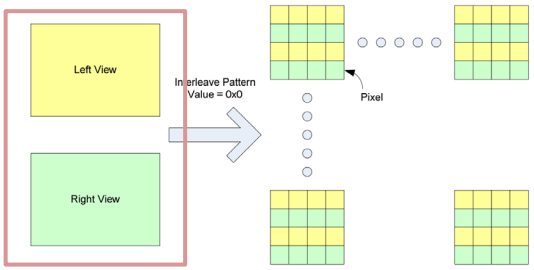


Figure 2-29: Interleave Pattern Corresponding to 2-way Interleaved Stereo where Right Image Pixels are on Even Lines

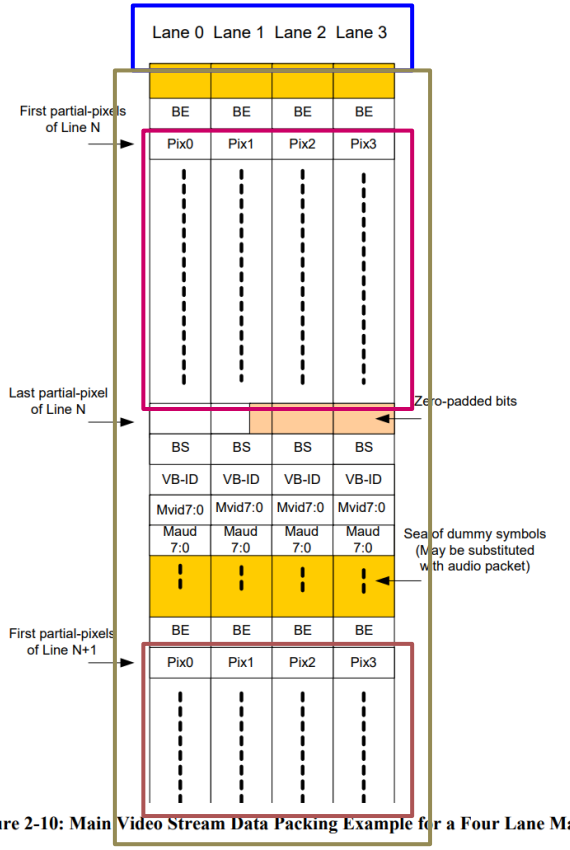
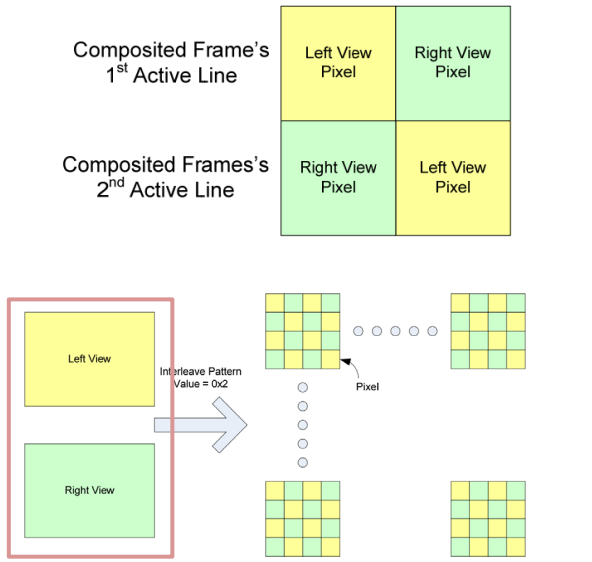
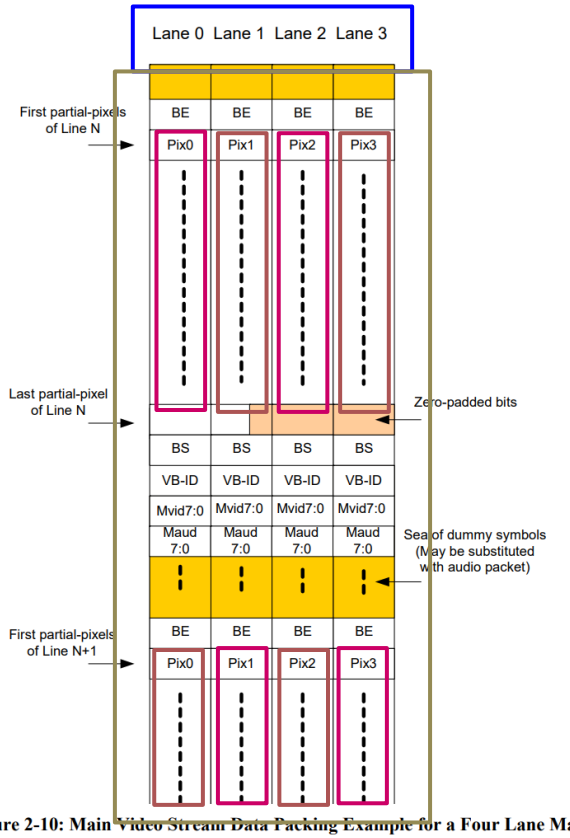


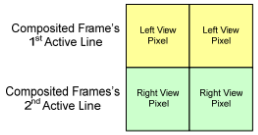
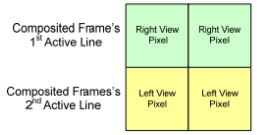
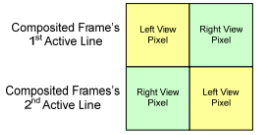
Figure 2-10: Main Video Stream Data Packing Example for a Four Lane Main Link

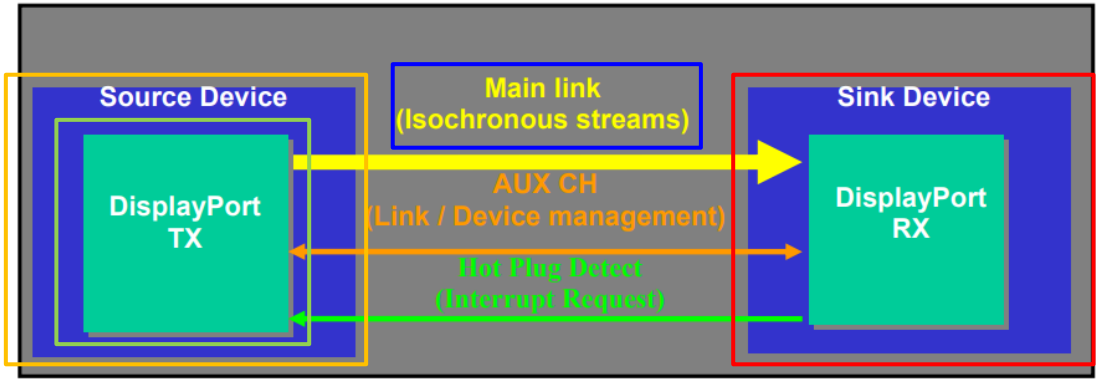
Claim 1	VESA DisplayPort Standard v1.2
a second mode to generate a stream of second data elements which carry a multiplexed combination of components of a stereoscopic image, wherein said components of said stereoscopic image elements being transmitted in a first portion of said interface and in a second portion of said interface,	***Value 0x2:*** Interleave pattern corresponding to a checkerboard pattern with alternating left and right view pixels starting with left view pixel. The corresponding 2x2 pattern is shown below:  Figure 2-30: Interleave Pattern Corresponding to 2-way Interleaved Stereo where Right Image Pixels are on Even Lines  Figure 2-10: Main Video Stream Data Packing Example for a Four Lane Main Link

Claim 1	VESA DisplayPort Standard v1.2
each of said first portion and said second portion having a lesser data carrying capacity than said known data carrying capacity and a combined data carrying capacity no greater than said known data carrying capacity,	**1.7.1 Make-up of the Main Link** The Main Link consists of one, two or four AC-coupled, doubly terminated differential pairs (called lanes). AC-coupling facilitates the silicon process migration since the DisplayPort transmitter and receiver may have different common mode voltages. The stream data is packed into "micro-packets" which are called "transfer units" in SST (Single Stream Transport) mode and MTP (Multi-stream Transport Packet) in MST (Multi-Stream Transport) mode. After the stream data is packed and mapped to main link, the packed stream data rate will be equal to or smaller than the link symbol rate of the main link. When it is smaller, stuffing symbols are inserted. **2.2.1.4 Symbol Stuffing and Transfer Unit** To avoid the oversubscription of the link bandwidth, the packed data rate must be equal to or lower than the link symbol rate. When the packed data rate is lower than the link symbol rate, the link layer must perform symbol stuffing. Stuffing symbols (both stuffing frame symbols and dummy data symbols) must be inserted in all lanes in the same LS_Clk cycle before inter-lane skewing. The dummy data symbols must be all 00h before scrambling. The dummy data symbols are inserted both between FS and FE, and between BS and BE.

Claim 1	VESA DisplayPort Standard v1.2
wherein the interface part is arranged to send signaling information across the interface, the signaling information identifying which mode the formatter is using and characteristics of said steam of second data elements.	**2.2.4 Main Stream Attribute Data Transport** This section describes the Main Stream attribute data that are transported for the reproduction of the main video stream by the Sink. The attribute data is sent once per frame during the vertical blanking period of the main video stream. Those attributes must be as follows: • Miscellaneous1 (MISC1, 8 bits) ▪ 00 = No 3D stereo video in-band signaling done using this field, indicating either no 3D stereo video transported or the in-band signaling done using an SDP called Video_Stream_Configuration (VSC) Packet ▪ 01 ▪ For progressive video, the next frame is RIGHT EYE ▪ For interlaced video, TOP field is RIGHT EYE and BOTTOM field is LEFT EYE ▪ 10 = RESERVED ▪ 11 ▪ For progressive video, the next frame is LEFT EYE ▪ For interlaced video, TOP field is LEFT EYE and BOTTOM field is RIGHT eye **2.2.5.6 Video_Stream_Configuration (VSC) Packet** A DP Source device may send 3D Stereo in-band signaling using VSC Packet by setting MSA Packet MISC1 field bits 2:1 to 00.

Claim 1	VESA DisplayPort Standard v1.2
wherein the interface part is arranged to send signaling information across the interface, the signaling information identifying which mode the formatter is using and characteristics of said steam of second data elements.	**2.2.5.6 Video_Stream_Configuration (VSC) Packet** A DP Source device may send 3D Stereo in-band signaling using VSC Packet by setting MSA Packet MISC1 field bits 2:1 to 00. **2.2.5.6.2 VSC Packet Payload** Table below shows the bit definitions of VSC Packet payload **Table 2-56: VSC Packet Payload** **DB0 bits 3:0 = Stereo Interface Method Code** / **DB0 bits 7:4 = Stereo Interface Method-Specific Parameter** 0 = Non Stereo Video — Must be set to 0x0 1 = Frame/Field Sequential (Figure 6, illustrates the composited frame format as transmitted by the source) — **Frame/Field Sequential Type:** ***Value 0x0:*** Left & Right view indication based on the MISC1 bit 2:1 ***Value 0x1:*** Right when Stereo Signal = 1 ***Value 0x2:*** Left when Stereo Signal = 1 All other values for this field (0x3-0xF) are RESERVED for future use. 2 = Stacked Frame (Figure 7, illustrates the composited frame format as transmitted by the source) — **Stacked Frame Type:** ***Value 0x0:*** Left view is on top and right view on bottom All other values for this field (0x1-0xF) are RESERVED for future use. 3 = Pixel Interleaved — **Interleave Pattern Type:** For interleave pattern type 1 through 4, a 2x2 pattern

Claim 1	VESA DisplayPort Standard v1.2
wherein the interface part is arranged to send signaling information across the interface, the signaling information identifying which mode the formatter is using and characteristics of said steam of second data elements.	grid (as shown in figure 2) is used to illustrate the interleaving pattern of the composited stereo frame. ***Value 0x0:*** Interleave pattern corresponding to 2-way horizontally interleaved stereo where right view pixels are on even lines. The corresponding 2x2 pattern is shown below:  ***Value 0x1:*** Interleave pattern corresponding to 2-way horizontally interleaved stereo where right view pixels are on odd lines. The corresponding 2x2 pattern is shown below:  ***Value 0x2:*** Interleave pattern corresponding to a checkerboard pattern with alternating left and right view pixels starting with left view pixel. The corresponding 2x2 pattern is shown below:  ***Value 0x3:*** Interleave pattern corresponding to 2-way vertically interleaved stereo starting with left view pixels. The corresponding 2x2 pattern is shown below: 4 = Side-by-side (Figure 5, illustrates the composited frame format and the timing requirement) Values 0x5-0xF are RESERVED Composited Frame's 1st Active Line Left View Pixel Right View Pixel Composited Frames's 2nd Active Line Left View Pixel Right View Pixel ***Value 0x4:*** Interleave pattern corresponding to 2-way vertically interleaved stereo starting with right view pixels. The corresponding 2x2 pattern is shown below: Composited Frame's 1st Active Line Right View Pixel Left View Pixel Composited Frames's 2nd Active Line Right View Pixel Left View Pixel All other values for this field (0x5-0xF) are RESERVED for future use. ***Value 0x0:*** A value of 0x0 indicate left half of the image represents left EYE view and right half represents right EYE view ***Value 0x1:*** A value of 0x1 indicate left half of the image represents right EYE view and right half represents left EYE view All other values for this field (0x2-0xF) are RESERVED for future use.

Claim 12	VESA DisplayPort Standard v1.2
12. A digital display interface part for use in an audio-visual device, said interface part supporting a digital display interface having a known data carrying capacity between the audio-visual device and a second audio-visual device, and receiving uncompressed pixel information, the interface part comprising:	**1.7 Overview of DisplayPort** A DisplayPort link consists of a main link, an auxiliary channel (AUX CH), and a Hot Plug Detect (HPD) signal line. **As shown in Figure 2-45: DisplayPort Data Transport Channels** below, the Main Link is a unidirectional, high-bandwidth and low-latency channel used below, the Main Link is a unidirectional, high-bandwidth and low-latency channel used to transport isochronous data streams such as uncompressed video and audio. The auxiliary channel is a half-duplex bidirectional channel used for link management and device control. The HPD signal also serves as an interrupt request by the Sink device. In addition, the DisplayPort connector for a box-to-box connection has a power pin for powering either a DisplayPort repeater or a DisplayPort-to-Legacy converter.  **Figure 1-1: DisplayPort Data Transport Channels**

Claim 12	VESA DisplayPort Standard v1.2
12. A digital display interface part for use in an audio-visual device, said interface part supporting a digital display interface having a known data carrying capacity between the audio-visual device and a second audio-visual device, and receiving uncompressed pixel information, the interface part comprising:	**1.7 Overview of DisplayPort** A DisplayPort link consists of a main link, an auxiliary channel (AUX CH), and a Hot Plug Detect (HPD) signal line. **As shown in Figure 2-45: DisplayPort Data Transport Channels** below, the Main Link is a unidirectional, high-bandwidth and low-latency channel used below, the Main Link is a unidirectional, high-bandwidth and low-latency channel used to transport isochronous data streams such as uncompressed video and audio. The auxiliary channel is a half-duplex bidirectional channel used for link management and device control. The HPD signal also serves as an interrupt request by the Sink device. In addition, the DisplayPort connector for a box-to-box connection has a power pin for powering either a DisplayPort repeater or a DisplayPort-to-Legacy converter. **1.7.1 Make-up of the Main Link** The Main Link consists of one, two or four AC-coupled, doubly terminated differential pairs (called lanes). AC-coupling facilitates the silicon process migration since the DisplayPort transmitter and receiver may have different common mode voltages. Three link rates are supported, 5.4Gbps, 2.7Gbps and 1.62Gbps per lane. All enabled lanes must be operating at the same link rate. The link rate is decoupled from the pixel rate. The pixel rate is regenerated from the link symbol clock using the time stamp values M and N. The capabilities of the DisplayPort transmitter and receiver, and the quality of the channel (or a cable) will determine whether the link rate is set to 5.4Gbps, 2.7Gbps or 1.62Gbps per lane.

Claim 12	VESA DisplayPort Standard v1.2
an input for receiving formatted image data from the interface;	

2.2.1 Main Stream to Main Link Lane Mapping in the Source Device

The Main Link must have one, two, or four lanes, with each lane capable of transporting eight bits of data per link symbol clock (LS_Clk). Main stream data (the uncompressed video stream) must be packed, stuffed, framed and, optionally, multiplexed with secondary-data and inter-lane skewed before it is handed over to the PHY layer after the Link Layer data mapping for transport over the main link. The stream data must enter the link layer at the original stream clock (Strm_Clk) rate and must be delivered to the PHY layer at the LS_Clk rate after this mapping.

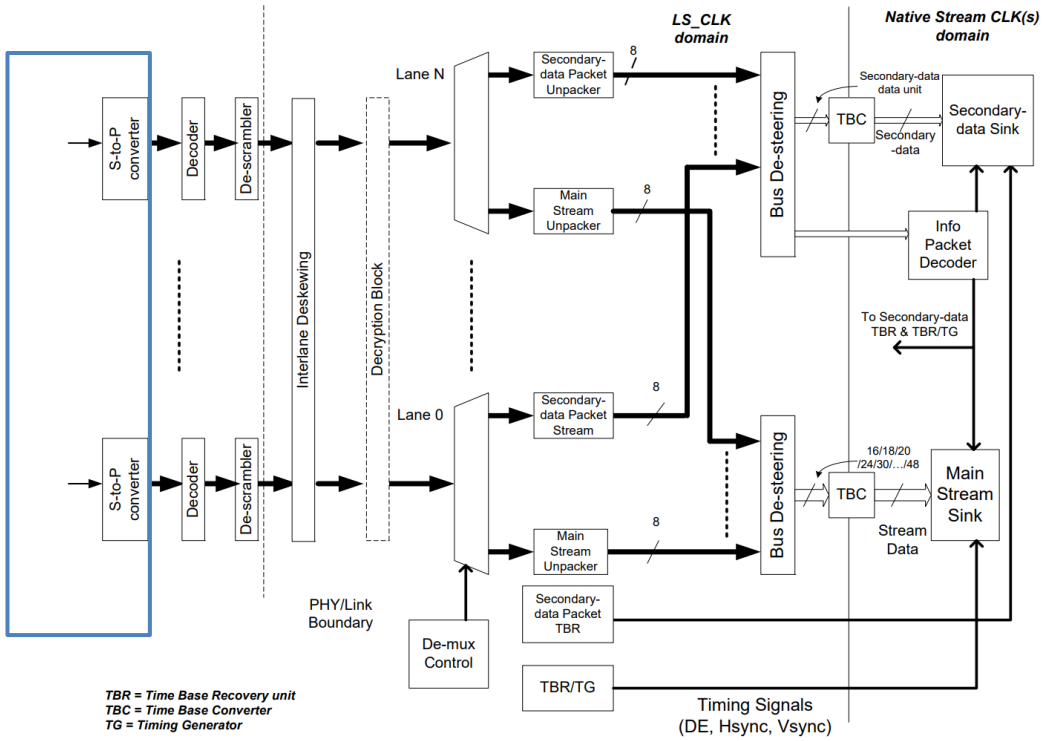


Figure 2-9: High Level Block Diagram of DP uPacket RX Main Link Data Path

Claim 12	VESA DisplayPort Standard v1.2
an input for receiving formatted image data from the interface;	

1.7.4 Layered, Modular Architecture

Figure 1-2: shows the layered architecture of DisplayPort.

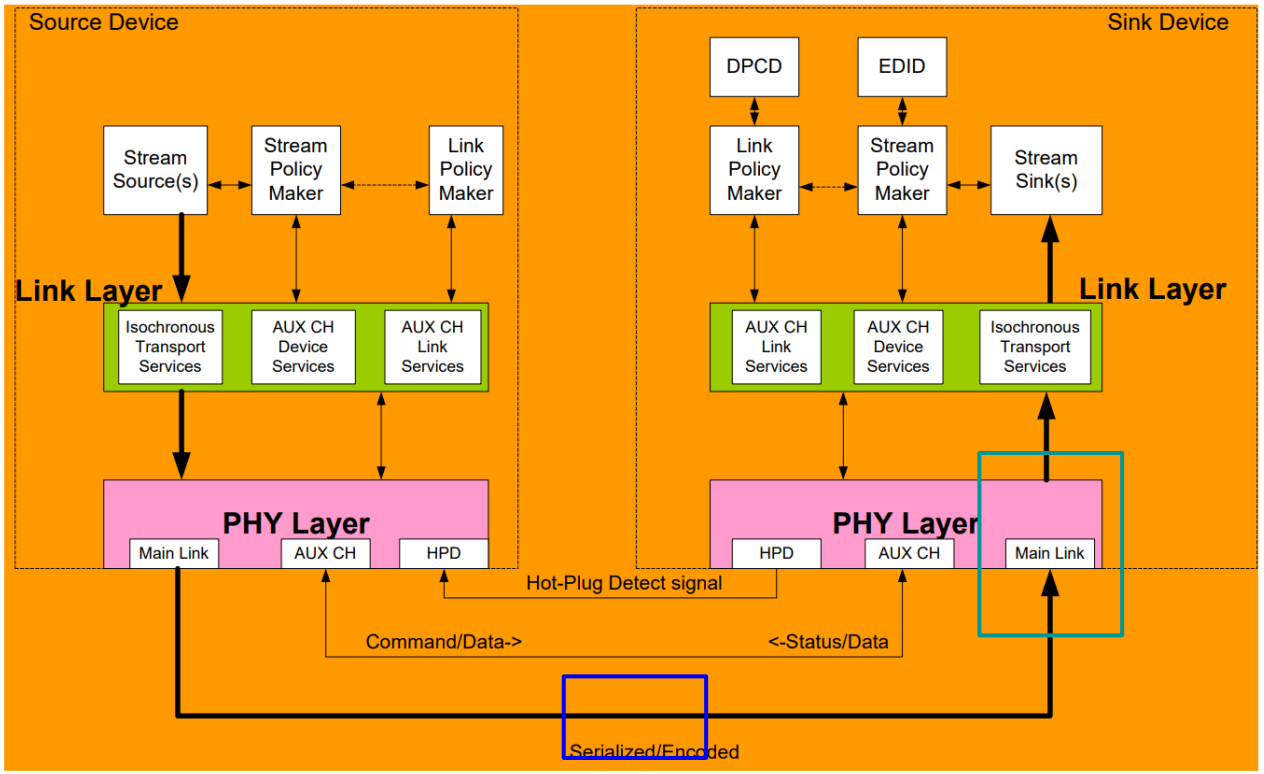


Figure 1-2: Layered Architecture

Claim 12	VESA DisplayPort Standard v1.2
a processor arranged to extract said image data, the processor being operable, in accordance with capabilities of said second audio-visual device, wherein	

2.2.1 Main Stream to Main Link Lane Mapping in the Source Device

The Main Link must have one, two, or four lanes, with each lane capable of transporting eight bits of data per link symbol clock (LS_Clk). Main stream data (the uncompressed video stream) must be packed, stuffed, framed and, optionally, multiplexed with secondary-data and inter-lane skewed before it is handed over to the PHY layer after the Link Layer data mapping for transport over the main link. The stream data must enter the link layer at the original stream clock (Strm_Clk) rate and must be delivered to the PHY layer at the LS_Clk rate after this mapping.

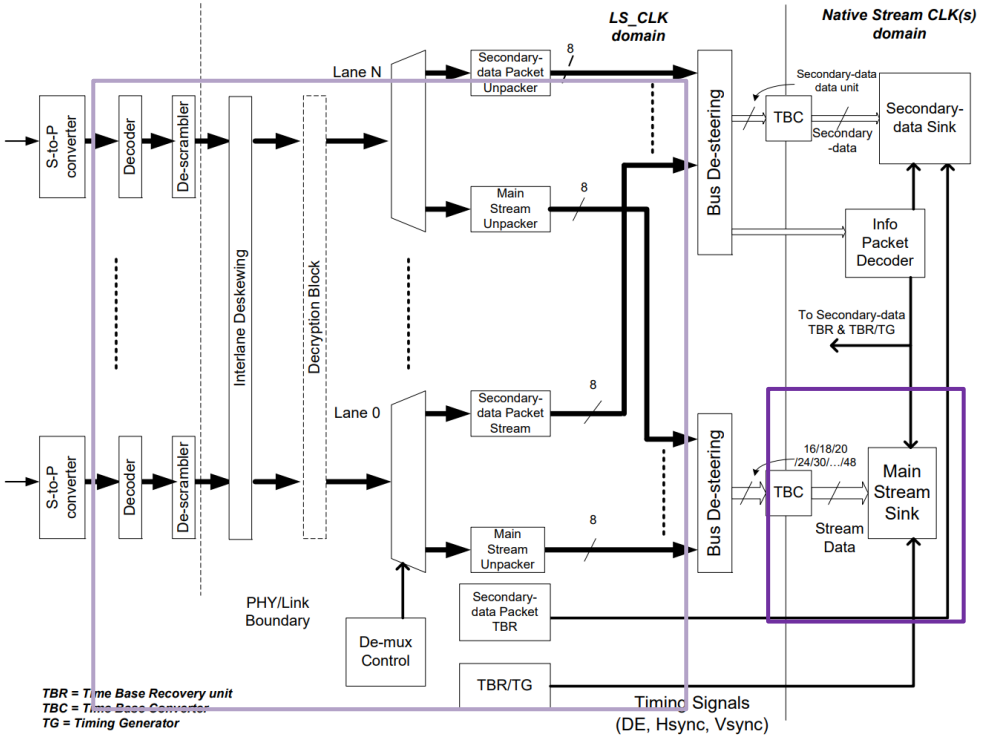


Figure 2-9: High Level Block Diagram of DP uPacket RX Main Link Data Path

Claim 12	VESA DisplayPort Standard v1.2
a processor arranged to extract said image data, the processor being operable, in accordance with capabilities of said second audio-visual device, wherein	**2 Link Layer** **2.1 SST Mode Introduction** This section describes the services provided by the link layer of DisplayPort in SST (single stream transport) mode. (Those sub-sections in this section that are applicable to both SST and MST modes are explicitly noted in the sub-section titles.) These services are: • Isochronous transport services over the main link The isochronous transport services, based on a micro-packet architecture, maps the video and audio streams onto the Main Link symbols with a set of rules, (explained in Section 2.2), so that the streams can be correctly re-constructed into the original format and time base in the Sink device.

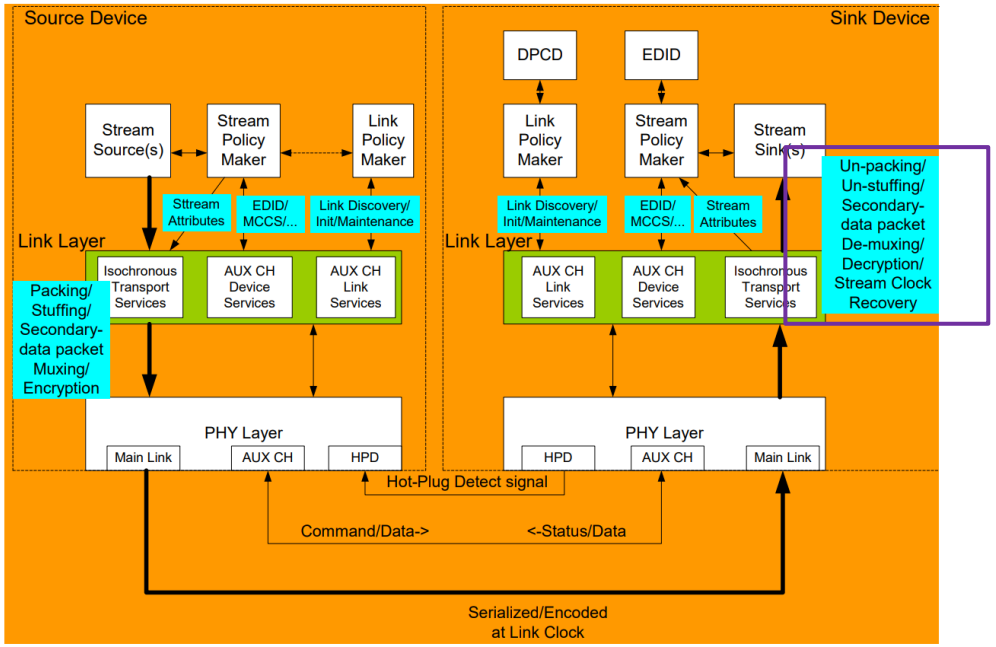
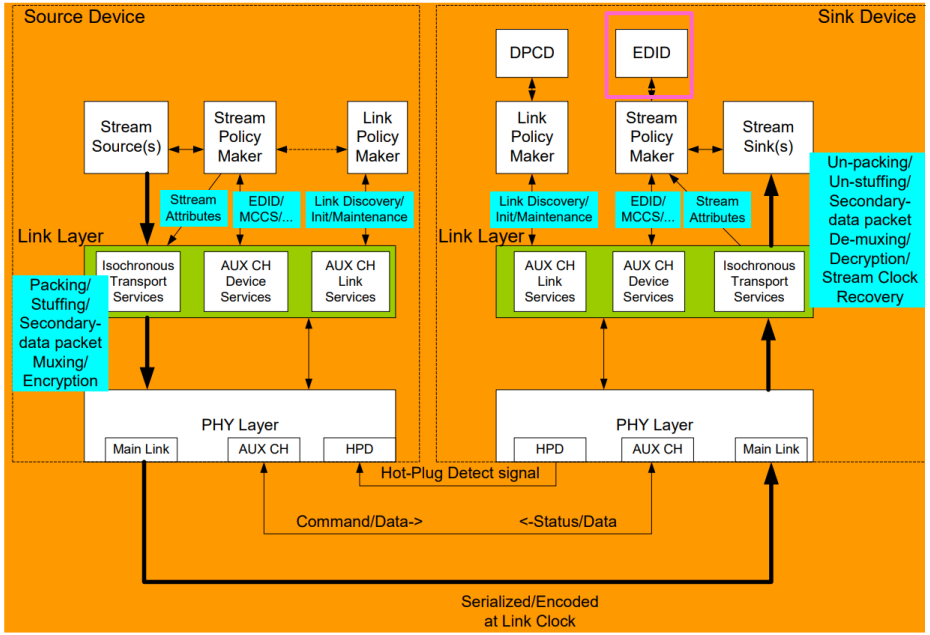


Figure 2-1: Overview of Link Layer Services

Claim 12	VESA DisplayPort Standard v1.2
a processor arranged to extract said image data, the processor being operable, in accordance with capabilities of said second audio-visual device, wherein	# 2 Link Layer ## 2.1 SST Mode Introduction This section describes the services provided by the link layer of DisplayPort in SST (single stream transport) mode. (Those sub-sections in this section that are applicable to both SST and MST modes are explicitly noted in the sub-section titles.) These services are: • Link and device management services over the AUX CH Link services are used for discovering, configuring, and maintaining the link. The AUX CH read/write access to DPCD (DisplayPort Configuration Data) address is used for these purposes. Device services support device-level applications such as EDID read and MCCS control. In addition, the AUX CH may be used for optional content protection.  **Figure 2-1: Overview of Link Layer Services**

Claim 12	VESA DisplayPort Standard v1.2
a processor arranged to extract said image data, the processor being operable, in accordance with capabilities of said second audio-visual device, wherein	

2.9.3.1 Address Mapping for Link Configuration/Management

Table 2-75 shows the DisplayPort address mapping for DPCD. The DPCD is byte addressed.

Table 2-75: Address Mapping for DPCD (DisplayPort Configuration Data)

DisplayPort Address	Definition	Read/Write over AUX CH
	Receiver Capability Field	
00000h	DPCD_REV : DPCD revision number Bits 3:0 = Minor revision number Bits 7:4 = Major revision number 10h for DPCD Rev.1.0 11h for DPCD Rev.1.1 12h for DPCD Rev 1.2 A DP device with uPacket RX with a DPCD Revision number of 1.2 and above must support GUID at DPCD Addresses 00030h ~ 0003Fh. Furthermore, a DP Sink device with DPCD Rev.1.2 with a stereo display capability support (as declared in EDID and Display ID) must support the handling of 3D Stereo in-band signaling using Video_Stream_Configuration (VSC) Packet. **Note:** The DPCD revision number does not necessarily match the DisplayPort version number.	Read Only

13 Appendix H: Protocol Support for 3D Stereo Display

13.2 3D Stereo Display Capability Declaration

The 3D stereo capability can be exposed in EDID and DisplayID. A 3D stereo format is usually associated with specific timing and hence it is desirable to indicate which timings support 3D stereo format and which don't. Furthermore, for a given timing that supports 3D stereo format it is required to indicate which stereo format is supported. Both EDID and DisplayID have the ability to expose 3D stereo capability per timing, but DisplayID provides for a more efficient and flexible format declaration.

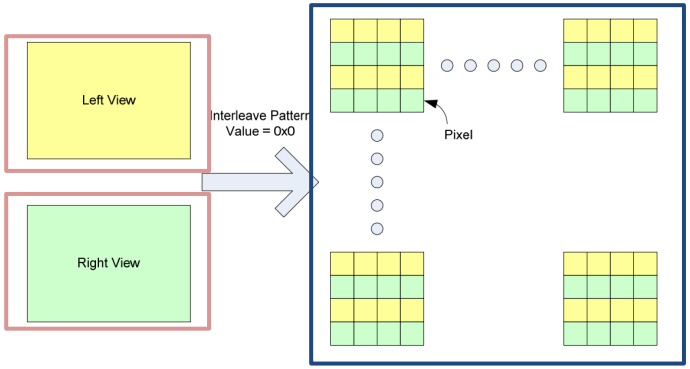
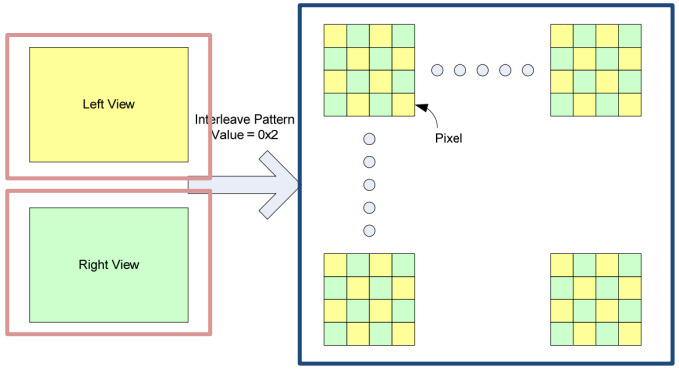
Claim 12	VESA DisplayPort Standard v1.2
in a first mode, the processor extracts pixel image data for a 2D image from a stream of first data elements at a data carrying capacity no greater than said known data carrying capability; and,	**2.2.4 Main Stream Attribute Data Transport** This section describes the Main Stream attribute data that are transported for the reproduction of the main video stream by the Sink. The attribute data is sent once per frame during the vertical blanking period of the main video stream. Those attributes must be as follows: • Miscellaneous1 (MISC1, 8 bits) o Stereo video attribute (bits 2:1) ▪ 00 = No 3D stereo video in-band signaling done using this field, indicating either no 3D stereo video transported or the in-band signaling done using an SDP called Video_Stream_Configuration (VSC) Packet **2.2.5.6 Video_Stream_Configuration (VSC) Packet** A DP Source device may send 3D Stereo in-band signaling using VSC Packet by setting MSA Packet MISC1 field bits 2:1 to 00. **2.2.5.6.2 VSC Packet Payload** Table below shows the bit definitions of VSC Packet payload **Table 2-56: VSC Packet Payload** **DB0 bits 3:0 = Stereo Interface Method Code** | **DB0 bits 7:4 = Stereo Interface Method-Specific Parameter** 0 = Non Stereo Video | Must be set to 0x0 **1.7.1 Make-up of the Main Link** The Main Link consists of one, two or four AC-coupled, doubly terminated differential pairs (called lanes). AC-coupling facilitates the silicon process migration since the DisplayPort transmitter and receiver may have different common mode voltages.

Claim 12	VESA DisplayPort Standard v1.2
in a first mode, the processor extracts pixel image data for a 2D image from a stream of first data elements at a data carrying capacity no greater than said known data carrying capability; and,	**1.7.1 Make-up of the Main Link** The Main Link consists of one, two or four AC-coupled, doubly terminated differential pairs (called lanes). AC-coupling facilitates the silicon process migration since the DisplayPort transmitter and receiver may have different common mode voltages. The stream data is packed into "micro-packets" which are called "transfer units" in SST (Single Stream Transport) mode and MTP (Multi-stream Transport Packet) in MST (Multi-Stream Transport) mode. After the stream data is packed and mapped to main link, the packed stream data rate will be equal to or smaller than the link symbol rate of the main link. When it is smaller, stuffing symbols are inserted. **2.2.1.4 Symbol Stuffing and Transfer Unit** To avoid the oversubscription of the link bandwidth, the packed data rate must be equal to or lower than the link symbol rate. When the packed data rate is lower than the link symbol rate, the link layer must perform symbol stuffing. Stuffing symbols (both stuffing frame symbols and dummy data symbols) must be inserted in all lanes in the same LS_Clk cycle before inter-lane skewing. The dummy data symbols must be all 00h before scrambling. The dummy data symbols are inserted both between FS and FE, and between BS and BE.

Claim 12	VESA DisplayPort Standard v1.2
in a second mode, the processor demultiplexes components of a stereoscopic image from a stream of second data elements which carry a multiplexed combination of components of a stereoscopic image,	**2.2.4 Main Stream Attribute Data Transport** This section describes the Main Stream attribute data that are transported for the reproduction of the main video stream by the Sink. The attribute data is sent once per frame during the vertical blanking period of the main video stream. Those attributes must be as follows: • Miscellaneous1 (MISC1, 8 bits) ○ Stereo video attribute (bits 2:1) ▪ 00 = No 3D stereo video in-band signaling done using this field, indicating either no 3D stereo video transported or the in-band signaling done using an SDP called Video_Stream_Configuration (VSC) Packet

Claim 12	VESA DisplayPort Standard v1.2
in a second mode, the processor demultiplexes components of a stereoscopic image from a stream of second data elements which carry a multiplexed combination of components of a stereoscopic image,	**2.2.5.6 Video_Stream_Configuration (VSC) Packet** A DP Source device may send 3D Stereo in-band signaling using VSC Packet by setting MSA Packet MISC1 field bits 2:1 to 00. **2.2.5.6.2 VSC Packet Payload** Table below shows the bit definitions of VSC Packet payload **Table 2-56: VSC Packet Payload**

DB0 bits 3:0 = Stereo Interface Method Code	DB0 bits 7:4 = Stereo Interface Method-Specific Parameter
1 = Frame/Field Sequential (Figure 6, illustrates the composited frame format as transmitted by the source)	**Frame/Field Sequential Type:** ***Value 0x0:*** Left & Right view indication based on the MISC1 bit 2:1 ***Value 0x1:*** Right when Stereo Signal = 1 ***Value 0x2:*** Left when Stereo Signal = 1 All other values for this field (0x3-0xF) are RESERVED for future use.
2 = Stacked Frame (Figure 7, illustrates the composited frame format as transmitted by the source)	**Stacked Frame Type:** ***Value 0x0:*** Left view is on top and right view on bottom All other values for this field (0x1-0xF) are RESERVED for future use.
3 = Pixel Interleaved	**Interleave Pattern Type:** For interleave pattern type 1 through 4, a 2x2 pattern

Claim 12	VESA DisplayPort Standard v1.2
in a second mode, the processor demultiplexes components of a stereoscopic image from a stream of second data elements which carry a multiplexed combination of components of a stereoscopic image,	**2.2.5.6 Video_Stream_Configuration (VSC) Packet** A DP Source device may send 3D Stereo in-band signaling using VSC Packet by setting MSA Packet MISC1 field bits 2:1 to 00.  **Figure 2-29: Interleave Pattern Corresponding to 2-way Interleaved Stereo where Right Image Pixels are on Even Lines**  **Figure 2-30: Interleave Pattern Corresponding to 2-way Interleaved Stereo where Right Image Pixels are on Even Lines**

Claim 12	VESA DisplayPort Standard v1.2
in a second mode, the processor demultiplexes components of a stereoscopic image from a stream of second data elements which carry a multiplexed combination of components of a stereoscopic image,	

2.2.5.6 Video_Stream_Configuration (VSC) Packet

A DP Source device may send 3D Stereo in-band signaling using VSC Packet by setting MSA Packet MISC1 field bits 2:1 to 00.

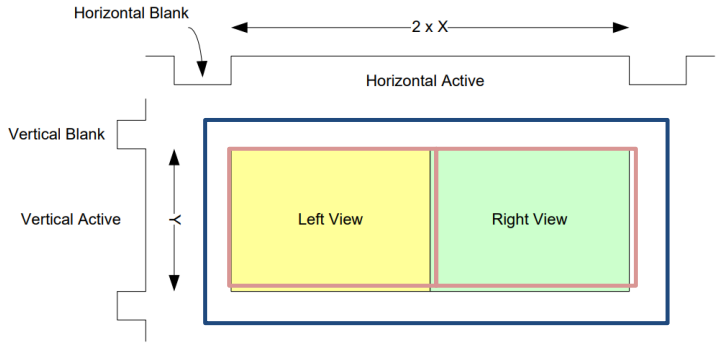


Figure 2-31: Interleave Pattern Corresponding to a Checkerboard Pattern with Alternating Left and Right Image Pixels

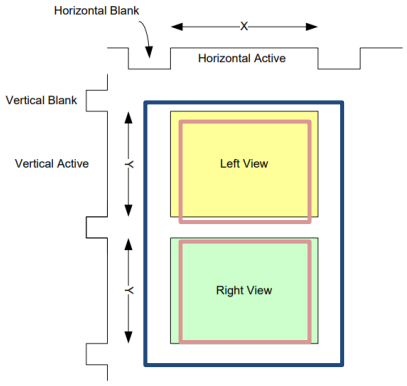


Figure 2-32: Field Sequential Stereo Format with Left View and Right View Indicated via MISC1 bits 2:1 Field of the MSA

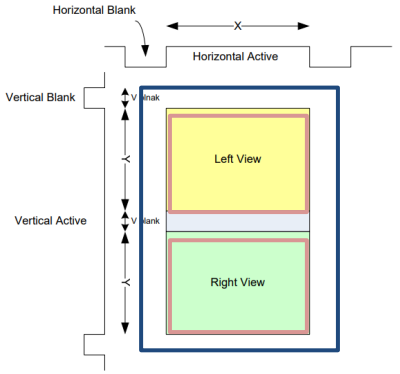


Figure 2-33: Stacked Top, Bottom Stereo Format with Left View on Top and Right View on Bottom

Claim 12	VESA DisplayPort Standard v1.2
wherein said components of said stereoscopic image elements being transmitted in a first portion of said interface and in a second portion of said interface,	**2.2.1.3 Main Video Stream Data Packing** The link layer must first steer pixel data in a pixel-within-lane manner as shown in Table 2-2. **Table 2-2: Pixel Steering into Main Link Lanes** <table><tr><th>Number of Lanes</th><th>Pixel Steering (N is 0 or positive integer)</th></tr><tr><td>4</td><td>Pixel 4N to lane 0 Pixel 4N+1 to lane 1 Pixel 4N+2 to lane 2 Pixel 4N+3 to lane 3</td></tr><tr><td>2</td><td>Pixel 2N to lane 0 Pixel 2N+1 to lane 1</td></tr><tr><td>1</td><td>All pixels to lane 0</td></tr></table>

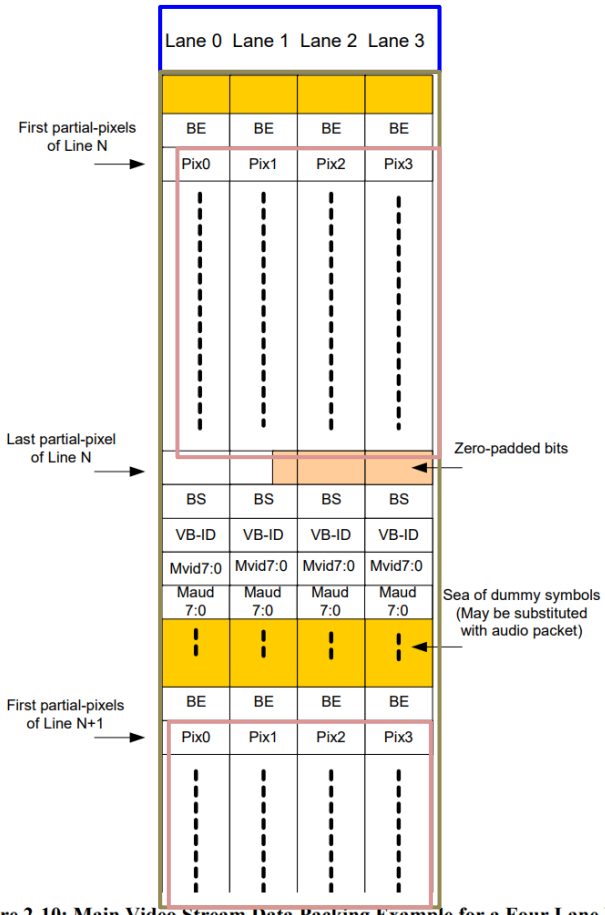
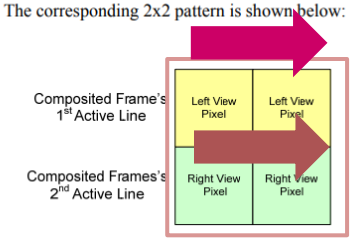
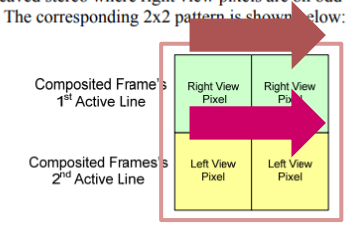
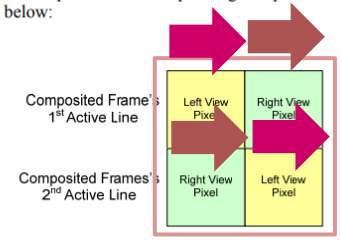
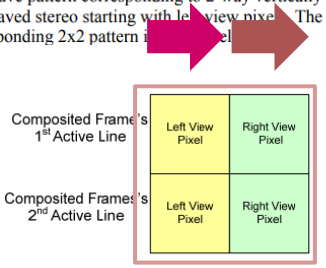
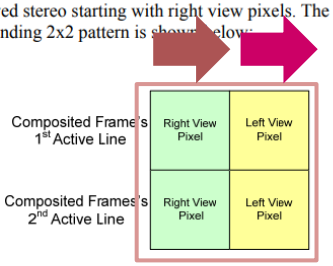
Claim 12	VESA DisplayPort Standard v1.2
wherein said components of said stereoscopic image elements being transmitted in a first portion of said interface and in a second portion of said interface,	

Figure 2-10: Main Video Stream Data Packing Example for a Four Lane Main Link

Claim 12	VESA DisplayPort Standard v1.2
wherein said components of said stereoscopic image elements being transmitted in a first portion of said interface and in a second portion of said interface,	**2.2.5.6 Video_Stream_Configuration (VSC) Packet** A DP Source device may send 3D Stereo in-band signaling using VSC Packet by setting MSA Packet MISC1 field bits 2:1 to 00. ***Value 0x0:*** Interleave pattern corresponding to 2-way horizontally interleaved stereo where right view pixels are on even lines. The corresponding 2x2 pattern is shown below:  ***Value 0x1:*** Interleave pattern corresponding to 2-way horizontally interleaved stereo where right view pixels are on odd lines. The corresponding 2x2 pattern is shown below:  ***Value 0x2:*** Interleave pattern corresponding to a checkerboard pattern with alternating left and right view pixels starting with left view pixel. The corresponding 2x2 pattern is shown below:  ***Value 0x3:*** Interleave pattern corresponding to 2-way vertically interleaved stereo starting with left view pixels. The corresponding 2x2 pattern is shown below:  ***Value 0x4:*** Interleave pattern corresponding to 2-way vertically interleaved stereo starting with right view pixels. The corresponding 2x2 pattern is shown below: 

Claim 12	VESA DisplayPort Standard v1.2
wherein said components of said stereoscopic image elements being transmitted in a first portion of said interface and in a second portion of said interface,	

2.2.5.6 Video_Stream_Configuration (VSC) Packet

A DP Source device may send 3D Stereo in-band signaling using VSC Packet by setting MSA Packet MISC1 field bits 2:1 to 00.

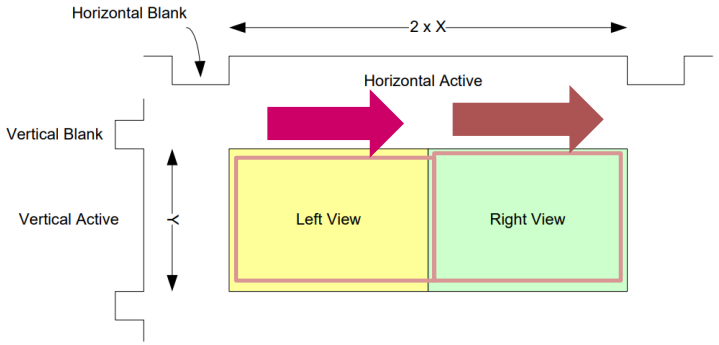


Figure 2-31: Interleave Pattern Corresponding to a Checkerboard Pattern with Alternating Left and Right Image Pixels

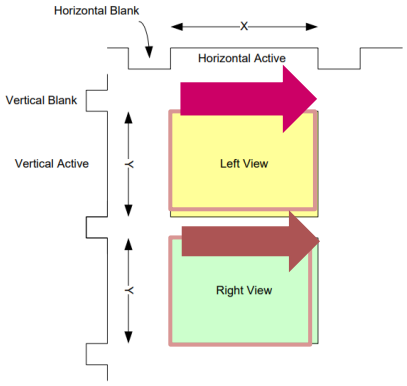


Figure 2-32: Field Sequential Stereo Format with Left View and Right View Indicated via MISC1 bits 2:1 Field of the MSA

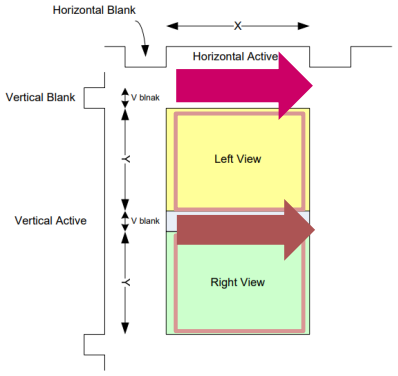


Figure 2-33: Stacked Top, Bottom Stereo Format with Left View on Top and Right View on Bottom

Claim 12	VESA DisplayPort Standard v1.2
wherein said components of said stereoscopic image elements being transmitted in a first portion of said interface and in a second portion of said interface,	

Value 0x0:
Interleave pattern corresponding to 2-way horizontally interleaved stereo where right view pixels are on even lines. The corresponding 2x2 pattern is shown below:

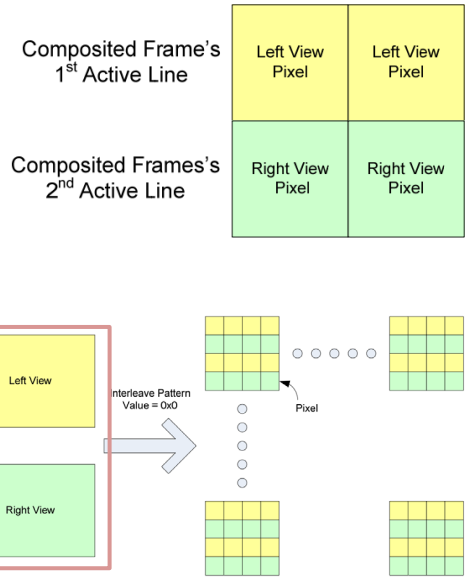


Figure 2-29: Interleave Pattern Corresponding to 2-way Interleaved Stereo where Right Image Pixels are on Even Lines

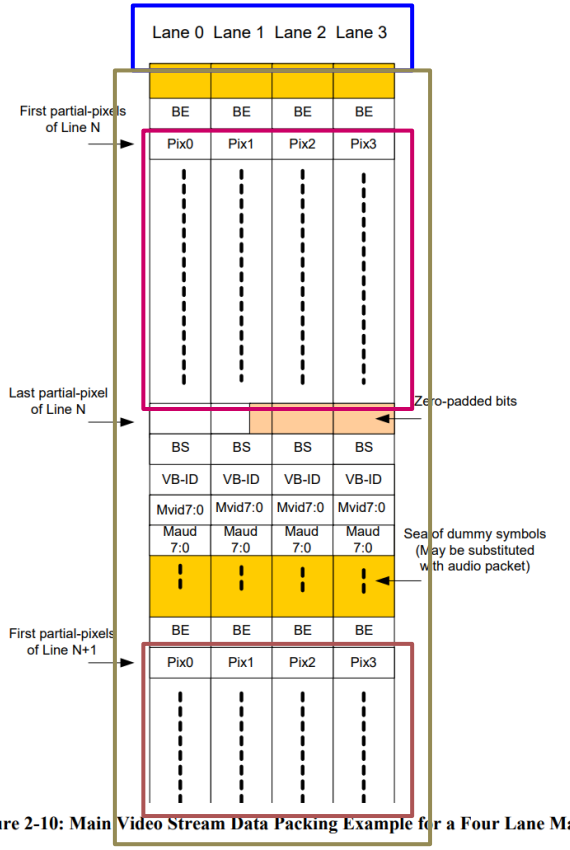
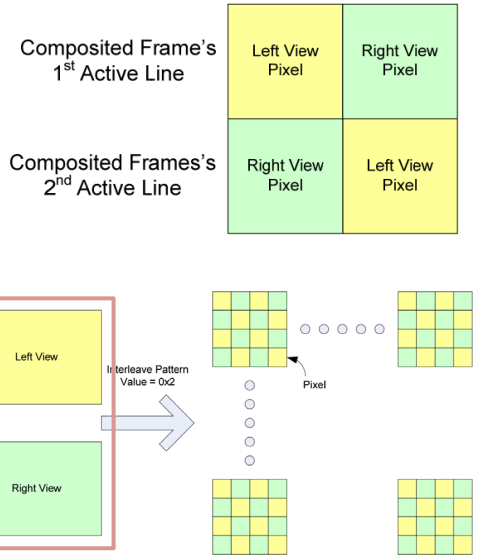
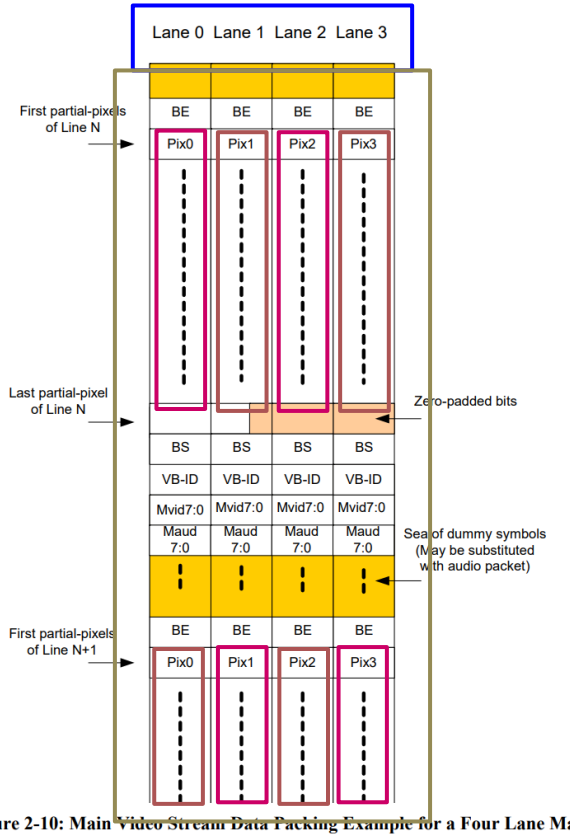


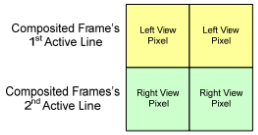
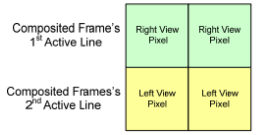
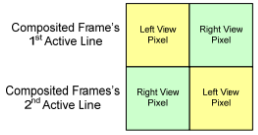
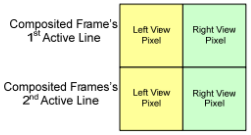
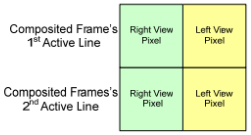
Figure 2-10: Main Video Stream Data Packing Example for a Four Lane Main Link

Claim 12	VESA DisplayPort Standard v1.2
wherein said components of said stereoscopic image elements being transmitted in a first portion of said interface and in a second portion of said interface,	***Value 0x2:*** Interleave pattern corresponding to a checkerboard pattern with alternating left and right view pixels starting with left view pixel. The corresponding 2x2 pattern is shown below:  Figure 2-30: Interleave Pattern Corresponding to 2-way Interleaved Stereo where Right Image Pixels are on Even Lines  Figure 2-10: Main Video Stream Data Packing Example for a Four Lane Main Link

Claim 12	VESA DisplayPort Standard v1.2
each of said first portion and said second portion having a lesser data carrying capacity than said known data carrying capacity and a combined data carrying capacity no greater than said known data carrying capacity,	**1.7.1 Make-up of the Main Link** The Main Link consists of one, two or four AC-coupled, doubly terminated differential pairs (called lanes). AC-coupling facilitates the silicon process migration since the DisplayPort transmitter and receiver may have different common mode voltages. The stream data is packed into "micro-packets" which are called "transfer units" in SST (Single Stream Transport) mode and MTP (Multi-stream Transport Packet) in MST (Multi-Stream Transport) mode. After the stream data is packed and mapped to main link, the packed stream data rate will be equal to or smaller than the link symbol rate of the main link. When it is smaller, stuffing symbols are inserted. **2.2.1.4 Symbol Stuffing and Transfer Unit** To avoid the oversubscription of the link bandwidth, the packed data rate must be equal to or lower than the link symbol rate. When the packed data rate is lower than the link symbol rate, the link layer must perform symbol stuffing. Stuffing symbols (both stuffing frame symbols and dummy data symbols) must be inserted in all lanes in the same LS_Clk cycle before inter-lane skewing. The dummy data symbols must be all 00h before scrambling. The dummy data symbols are inserted both between FS and FE, and between BS and BE.

Claim 12	VESA DisplayPort Standard v1.2
the interface part further arranged to receive signaling information across the interface, the signaling information identifying which of said first mode and said second mode is used and characteristics of said steam of second data elements.	**2.2.4 Main Stream Attribute Data Transport** This section describes the Main Stream attribute data that are transported for the reproduction of the main video stream by the Sink. The attribute data is sent once per frame during the vertical blanking period of the main video stream. Those attributes must be as follows: • Miscellaneous1 (MISC1, 8 bits) ▪ 00 = No 3D stereo video in-band signaling done using this field, indicating either no 3D stereo video transported or the in-band signaling done using an SDP called Video_Stream_Configuration (VSC) Packet ▪ 01 ▪ For progressive video, the next frame is RIGHT EYE ▪ For interlaced video, TOP field is RIGHT EYE and BOTTOM field is LEFT EYE ▪ 10 = RESERVED ▪ 11 ▪ For progressive video, the next frame is LEFT EYE ▪ For interlaced video, TOP field is LEFT EYE and BOTTOM field is RIGHT eye **2.2.5.6 Video_Stream_Configuration (VSC) Packet** A DP Source device may send 3D Stereo in-band signaling using VSC Packet by setting MSA Packet MISC1 field bits 2:1 to 00.

Claim 12	VESA DisplayPort Standard v1.2
the interface part further arranged to receive signaling information across the interface, the signaling information identifying which of said first mode and said second mode is used and characteristics of said steam of second data elements.	**2.2.5.6 Video_Stream_Configuration (VSC) Packet** A DP Source device may send 3D Stereo in-band signaling using VSC Packet by setting MSA Packet MISC1 field bits 2:1 to 00. **2.2.5.6.2 VSC Packet Payload** Table below shows the bit definitions of VSC Packet payload **Table 2-56: VSC Packet Payload** **DB0 bits 3:0 = Stereo Interface Method Code** / **DB0 bits 7:4 = Stereo Interface Method-Specific Parameter** 0 = Non Stereo Video — Must be set to 0x0 1 = Frame/Field Sequential (Figure 6, illustrates the composited frame format as transmitted by the source) — **Frame/Field Sequential Type:** ***Value 0x0:*** Left & Right view indication based on the MISC1 bit 2:1 ***Value 0x1:*** Right when Stereo Signal = 1 ***Value 0x2:*** Left when Stereo Signal = 1 All other values for this field (0x3-0xF) are RESERVED for future use. 2 = Stacked Frame (Figure 7, illustrates the composited frame format as transmitted by the source) — **Stacked Frame Type:** ***Value 0x0:*** Left view is on top and right view on bottom All other values for this field (0x1-0xF) are RESERVED for future use. 3 = Pixel Interleaved — **Interleave Pattern Type:** For interleave pattern type 1 through 4, a 2x2 pattern

Claim 12	VESA DisplayPort Standard v1.2
the interface part further arranged to receive signaling information across the interface, the signaling information identifying which of said first mode and said second mode is used and characteristics of said steam of second data elements.	grid (as shown in figure 2) is used to illustrate the interleaving pattern of the composited stereo frame. ***Value 0x0:*** Interleave pattern corresponding to 2-way horizontally interleaved stereo where right view pixels are on even lines. The corresponding 2x2 pattern is shown below:  ***Value 0x1:*** Interleave pattern corresponding to 2-way horizontally interleaved stereo where right view pixels are on odd lines. The corresponding 2x2 pattern is shown below:  ***Value 0x2:*** Interleave pattern corresponding to a checkerboard pattern with alternating left and right view pixels starting with left view pixel. The corresponding 2x2 pattern is shown below:  ***Value 0x3:*** Interleave pattern corresponding to 2-way vertically interleaved stereo starting with left view pixels. The corresponding 2x2 pattern is shown below:  ***Value 0x4:*** Interleave pattern corresponding to 2-way vertically interleaved stereo starting with right view pixels. The corresponding 2x2 pattern is shown below:  All other values for this field (0x5-0xF) are RESERVED for future use 4 = Side-by-side (Figure 5, illustrates the composited frame format and the timing requirement) ***Value 0x0:*** A value of 0x0 indicate left half of the image represents left EYE view and right half represents right EYE view ***Value 0x1:*** A value of 0x1 indicate left half of the image represents right EYE view and right half represents left EYE view All other values for this field (0x2-0xF) are RESERVED for future use. Values 0x5-0xF are RESERVED